AF/2133 JHW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:		
Inventors:	Castagnozzi et al.	
Serial No.:	10/020,426	ATTORNEY FILE NO. applied_114
Filed:	December 7, 2001	
Title:	SYSTEM AND METHOD FOR NON-CAUSAL CHANNEL EQUALIZATION	Confirmation No. 9539
		Examiner: Joseph D. Torres
		Customer No. 29397
		Art Unit 2133

CERTIFICATION UNDER 37 CFR § 1.8

I hereby certify that the documents referred to as enclosed herein are being deposited with the United States Postal Service as first class mail on this date 4/27/2005, in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

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Enclosed is an Appeal Brief for the above-reference application, a check to cover the Appeal Brief fee, and a return receipt postcard.

Respectfully submitted,

Date: 4/26/05

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THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF APPEALS

In re Application of: Castagnozzi et al.	Group Art Unit: 2133
Serial No. 10/020,426	Examiner: Joseph D. Torres
Filed: December 7, 2001	Docket No.: applied_114
For: SYSTEM AND METHOD FOR NON-CAUSAL CHANNEL EQUALIZATION	Customer No.: 29397
	Confirmation No.: 9539

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

BRIEF ON APPEAL

This is an appeal from the rejection by Examiner Joseph D. Torres, Group Art Unit 2133, of claims 17-48 as set forth in the CLAIMS APPENDIX.

REAL PARTY IN INTEREST

The real party in interest is Applied Microcircuits Corporation, as assignee of the present application by an Assignment in the United States Patent Office with a Recordation Date of February 12, 2002, at Reel 012582, Frame 0915.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF THE CLAIMS

Claims 17-48 are in the application.

Claims 17, 33, and 35 are rejected.

Claims 17-48 are appealed.

STATUS OF AMENDMENTS

Amendments were made to the claims in an Office Action response received at the PTO on February 14, 2005. These claim amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

An explanation of the problem addressed by the claimed invention occurs in the specification at page 1, ln. 10 through page 2, ln. 23 (see Attachment A). The invention addresses the issue of dispersion compensation in the interpretation of a serial stream of data bits. A "1" or a

"0" binary data bit is conventionally interpreted against a threshold voltage, which may be the median voltage between voltage extremes. That is, 2.5 volts may be the threshold in a system that uses +5 voltages and ground as a reference. The present invention minimizes interpretation errors by adjusting the decision threshold. The adjustment of the threshold is based upon the understanding that the optimal threshold depends upon the pattern of serial bits being received. In a series of three binary bits for example, there are eight possible patterns. They are: 111, 011, 101, 110, 001, 100, 010, and 000. If the bits immediately preceding and following a current (unknown) bit have been determined to be "1s" (1 ? 1), then the average DC voltage of the stream will be higher than if the preceding/following bits are "0s" (0 ? 0). Knowing that the average voltage changes in response to the serial bit pattern, the decision thresholds can be adjusted to improve accuracy.

Please refer to Fig. 3 (Attachment B), and to the description at page 6, line 12 through page 7, line 13, for an explanation of the present invention non-causal channel equalization circuit. A multi-threshold circuit 102 generates a plurality of estimates (3 estimates are shown) in response to each received bit. Generally, the estimates are made against a mid-voltage threshold (Vopt), a high voltage threshold (V1), and a low voltage threshold (V0). For the current clock cycle, the non-causal circuit 110 compares a first bit estimate (described in the next paragraph), to bit values determined in other (non-current) clock cycles, to generate a (first) bit value for the current clock cycle.

As described on page 14, ln. 3 through page 15, ln. 25, a future circuit 114 (see Fig. 7A) performs two functions. It uses the mid-voltage estimate (Vopt) 120c, which is similar to a conventional decision threshold,

to determine the subsequent (third) bit value. The future decision circuit also compares the three threshold outputs to generate the first bit estimate. The first bit estimate is represented by the combination of lines 120a and 120b. The past decision circuit 116 supplies the bit value from the previous clock cycle (second bit value) on line 118. The present decision circuit compares the first bit estimate (120a/120b) to the third bit value (120c) and the past bit value (118).

The truth table of Fig. 7B shows the first bit value obtained in response to comparing the first bit estimate to the past (2^{nd}) and next (3^{rd}) bit values. The first four lines of the Table represent the simple case where the received signal is measured to be less than the low threshold V0 (lines 108a, 108b, and 108c are all "0"), see Fig. 3. Regardless of the 2^{nd} and 3^{rd} bit values, the current (1^{st}) bit value is determined to always be a "0". Likewise, the last four lines represent the simple case where the received signal is measured to be greater than V1. In this scenario, the first bit is always "1". The second set of four lines represent a more interesting case where the received signal is measured to be above the low threshold V0, but below the mid-threshold Vopt. In this case, the first estimate (120a/120b) is represented in the Table as "0, 1". If either, or both of the 2^{nd} or 3^{rd} bits is a "1", a decision is made that essentially raises the overall threshold, and the 1^{st} bit is determined to be a "0". If the 2^{nd} and 3^{rd} bits are both "0", then a lower overall threshold is used, and the 1^{st} bit is determined to be a "1". The third set of four lines is the case where the received signal is measured to be above the mid-threshold Vopt, but below the high threshold V1. If either, or both of the 2^{nd} or 3^{rd} bits is a "0", the 1^{st} bit is determined to be a "1". If the 2^{nd} and 3^{rd} bits are both "1", then a higher overall threshold is

used, and the 1st bit is determined to be a "0". A more graphic depiction of the decision making process is shown in Fig. 4.

In some aspects (claim 35), forward error corrections (FEC) may be used to adjust the V0, V1, and Vopt threshold values.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether Claims 17, 33, and 35 are unpatentable under 35 U.S.C. 103(a) with respect to Andresen et al. ("Andresen"; US 3,670,304), in view of Abe et al. ("Abe"; US 5,781,588).

ARGUMENT

The Rejection of claims 17, 33, and 35 as unpatentable under 35 U.S.C. 103(a) with respect to Andresen et al. ("Andresen"; US 3,670,304), in view of Abe et al. ("Abe"; US 5,781,588).

With respect to claims 17 and 33, the Office Action states that Andresen describes a multi-threshold decision circuit that provides bit estimates, and a non-causal circuit to supply a bit value for a current bit estimate in response to a non-causal analysis. The Office Action acknowledges that Andresen does not teach the use of non-return to zero (NRZ), but states that it would have been obvious apply Abe's NRZ data format to Andresen, to make the claimed invention obvious. With respect the claim 35, the Office Action states that Andresen's parity check circuit 94 and error correction circuit 96 are an FEC circuit. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

The Final Office Action (page 7) equates Andresen's Amplitude Sense and Data Gate circuit 20 with the Applicant's multi-threshold circuit. However, Andresen does not describe a circuit that provides multiple estimates in response to each data input. Andresen describes a system that includes a read head 10 to detect an analog signal. A read amplifier 12 hard-limits the received signal, to create a 2-level (high or low voltage) signal. Andresen mentions that either a high or a low threshold may be used to control AND gate 16 (col. 3, ln. 68-75), and a "zero level" threshold can be used by OR gate 18 (col. 4, ln. 1-17). The two series-connected thresholds are shown as trace "B" (line 22 of Fig. 1) and "C" (line 44 of Fig. 1) in Fig. 2. The composite threshold is shown as signal "D" (Fig. 2) and the output on line 27 (Fig. 1) is shown as signal "E" (Fig. 2). The explanation of Fig. 2 also states that when the amplitude of the digital signal deteriorates, the system reverts back to the analog signal (col. 5. ln. 72 through col. 6, ln 8). Andresen also describes circuitry

that is used to create the limiting thresholds. In short, Andresen describes a system that hard-limits analog data using a composite threshold, and uses feedback to control the limiting thresholds.

In the *Response to the Arguments* Section of the Final Office Action (bottom of page 2), the Examiner states Andresen provides estimates of the analog signal, to resolve the analog signal into a digital signal. However, assuming for the sake of argument that the hard-limited signal is a bit estimate, it still does not describe the claimed invention. Claims 17, 33, and 35 recite that the multi-threshold circuit outputs a plurality of bit estimates for each (input) data. Andresen shows only a single hard-limited signal for each data input (tape track), although there can be up to 9 parallel inputs (tracks), see Andresen Fig. 3. In this case, Andresen generates nine estimates, one for each of the nine inputs.

The Final Office Action (page 7) also equates Andresen's comparators 138 and 124 in Figs. 6 and 7, with the Applicant's non-causal circuit. Andresen describes this circuitry as a Data Detector, which is block 28 of Fig. 1. The hard-limited input signal (line 28 in Fig. 1 and "A" in Fig. 6) is the input to the data detector. In the data detector (Fig. 6), the hard-limited signal is converted to narrow pulses and ANDed with the clock pulses. The result is sent to a one-shot 116, to create the data pulses "C" (Fig. 7) (col. 8, ln. 17-36).

Comparator 124 generates the clock pulse ("E" in Fig. 7) from a sawtooth, RC time constant input waveform (col. 8., ln. 37-49). Comparator 138 is used to detect phase error by monitoring waveform "D". If the "D" pulse is too long, a pulse is generated and sent to the phase error latch; block 26 of Fig. 1 (col. 9, ln. 1-23). The final clock pulse is waveform "E" (Fig. 7).

The clock pulse ("E", Fig. 7)) is fed back to AND gates 132 and 134. This ANDed output is, in turn, ANDed (118) with the data pulses ("C", Fig. 7) to generate the "1s" data waveform "G" (col. 8, ln. 61-75).

In comparing Andresen to the claimed non-causal circuit, the Office Action (page 7) states that, "bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles". However, Andresen's comparators 124 and 138 generate clock pulses and phase errors, respectively. The constant amplitude voltage levels associated with R1 and R2 can be clearly seen in Fig. 7. Since R1 and R2 are merely dc voltages used to generate clock and phase information, they cannot represent "bit values determined in non-current clock cycles", as recited in the Applicant's claims.

The Office Action (last paragraph of page 8) states that Andresen's XOR circuit 112 receives a current bit estimate "A" and a previous bit estimate "A" from delay 110. The Office Action asserts that the output of delay 110 is a bit value from a non-current clock cycle that is being compared to a current clock cycle estimate. However, this analysis is incorrect in a number of respects. XOR 112 compares an input pulse ("A") to a delayed version of the same pulse. In this manner, narrow pulses ("B") are created that are associated with the rising and falling edges of the "A" pulses. Andresen states that, "(t)he digital signal is converted into a pulse signal for each transition by delay 110 and exclusive OR 112." (col. 8, ln. 19-21). These "B" pulses are an input in the creation of the data pulses "C". The Applicant respectfully submits that Andresen's gate delays are being confused with clocked data bits.

The claimed invention recites comparing a bit estimate for a current clock cycle to bit values determined in non-current clock cycles. As described above in the Applicant's explanation of Andresen's circuit (above), Andresen generates a clock ("E") from the input data. The only clocked data pulse generated by Andresen ("G"), occurs as a result of comparing clock waveform "E" to data waveform "C". Further, this waveform "G" is only a waveform of clocked "1s" data. Nowhere does Andresen describe clocked data pulses "G" being used in the analysis of any subsequently received waveforms. Since Andresen does not show waveform "G" being compared to the subsequent input "A", he does teach the claimed invention non-causal circuit.

Abe describes 51 variations of an FSK demodulator (col. 1, ln. 35 through col. 10, ln. 39). A frequency converter converts the received signal to a second frequency, lower that the first (received) frequency. The second frequency signal is demodulated to baseband. The baseband signal is compared to a threshold, and the number of threshold crossings is counted. In the embodiment mentioned at col. 23, ln. 42-46 (Fig. 18), the baseband signal is said to be in NRZ format.

With respect to the first *prima facie* requirement to support a case of obviousness, there must be a motivation, either in the references or in the general art, to combine the references in such as way as to make the claimed invention obvious. The Office Action states (page 9) that with respect to claims 17, that it would have been obvious to apply the teaching of Abe (NRZ coding) to Andresen, since Andresen's circuit is designed "to resolve and reproduce digital data and NRZ encoded data is digital data..." The Office Action also states that "one of ordinary skill in the art would have recognized that the use of non-return to zero NRZ would have

provided the opportunity to apply the teachings in the Andresen patent to the specific type of data for which it was designed such as NRZ which is a widely used for of encoding for magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe)."

In the *Response to the Arguments* Section (page 4), the Examiner states that motivation to combine references is based upon the fact that the IEEE Dictionary defines NRZ as a format associated with magnetic tapes. The Applicant respectfully submits that this analysis is incomplete. Prior art references cannot be combined for the purposes of an obviousness analysis merely on the basis of a retrospective desire to combine different subject matter. Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion of motivation in the references to do so." *In re Mills*, 916 F.2d 680, 682, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990). Here, the analysis must determine if there is any motivation in the Abe reference to modify Andresen in such way as to make the claimed invention obvious. The Applicant respectfully submits no evidence has been supplied showing that Abe, or the knowledge generally available in the art, supplies such motivation. In summary, the Applicant respectfully submits that a *prima facie* case for supporting a motivation to combine references has not been made.

With respect to the second *prima facie* obviousness requirement, even if the references are combined, there is no reasonable expectation of success. That is, even if an expert where given the Andresen and Abe inventions as a foundation, it is unlikely that they could come up with a circuit that supplies multiple bit estimates for each

input data, or a circuit that make a bit value decision based upon a comparison of a current clock cycle bit estimate, with bit values decided in non-current clock cycles.

In the *Response to the Arguments* Section of the Office Action (page 5), the Examiner states that no modifications need be performed upon the Andresen circuitry to process NRZ data, and that the Abe reference was merely introduced to show that the NRZ format is well known. In response, the Applicant respectfully submits that the processing of NRZ data is not the most relevant factor in the analysis, as the Andresen reference fails to teach either a multi-threshold circuit or a non-causal circuit. Rather, the analysis must support how an expert could modify Andresen, using Abe or well-known information, to yield the elements of the claimed invention. However, no analysis has been performed to show how an expert could be expected to change Andresen's hard-limiter into a multi-threshold circuit. Neither is there any analysis of how Andresen's conventional self-clocking data circuit could be modified to use the decisions made in non-current clock cycles to influence the current clock cycle decision.

The combination of references most clearly fails to support the third *prima facie* requirement, as the combination does not teach all the limitations of the invention of claims 17, 33, and 35. First, the claimed invention recites a multi-threshold circuit that provides a plurality of bit estimates for each (input) data. The Applicant submits that neither Andresen nor Abe generate a plurality of bit estimates for each data input. Even if Andresen's hard-limited signal could be considered to be a bit estimate, Andresen supplies only a single "estimate" for each input (tape track). Further, neither Andresen nor Abe describes a

circuit that compares a current clock cycle estimate to bit values that were decided in other (non-current) clock cycles. Therefore, neither Andresen nor Abe teach a non-causal circuit.

With respect to claim 35, neither Andresen nor Abe describe an FEC circuit that generates the threshold levels used by the multi-threshold circuit. The Final Office Action states that Andresen's parity check circuit 94 and error correction circuit 96 are an FEC circuit (Fig. 3). However, even if Andresen does describe an error correction circuit, his circuit is not used in the generation of any threshold levels. More specifically, Andresen does not use an FEC circuit to generate multiple threshold levels for a multi-threshold circuit, as recited in the claimed invention.

The Applicant's Office Action response dated February 14, 2005 included the affidavit of Dr. Oswin Schreiber, enclosed herein as Attachment E. A partial list of Dr. Schreiber's publications is enclosed as Attachment F. The affidavit was prepared to rebut the obviousness rejections made by the Examiner. More fundamentally, the affidavit was prepared to bolster the Applicant's descriptions of the prior art. Dr. Schreiber's description of the Andresen patent generally confirms the Applicant's explanations, and is at odds with the descriptions presented in the Office Action.

Dr. Schreiber notes some fundamental differences between Andresen and the claimed invention. Andresen attempts to optimize a received signal by hard-limiting the signal. The claimed invention, on the other hand, optimizes the received signal by refining the measurement process. The input signal is measured against a plurality of thresholds, creating a corresponding plurality of estimates. Dr. Schreiber maintains

that Andresen does not generate a plurality of estimates for each input signal, even if the hard-limited signal is interpreted as an estimate.

Further, Dr. Schrieber states that Andresen does not compare a current clock cycle estimate to bit value decisions made in non-current clock cycles.

Section 716.01(a) of the MPEP states that affidavits presented to rebut obviousness rejections must be considered by the Examiner, *Stratoflex, Inc., v. Aeroquip Corp*, 713 F.2d 1530, 1538, 218 USPQ 871, 879 (Fed. Cir. 1983). Further, "(i)f, after evaluating the evidence, the examiner is not convinced that the claimed invention is patentable, the next Office action should include a statement to that effect and identify the reason(s)..." *Demaco Corp. v F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 7 USPQ2d 1222 (Fed. Cir.) However, the Examiner in this case has failed to consider or address any of the points raised by Dr. Schrieber. As an expert in the field, Dr. Schreiber is likely to have to best understanding of all the involved parties, as to how the Andresen and claimed invention circuitry operates. As a result, Dr. Schreiber statements are dispositive to the issue of whether Andresen actually describes the multi-threshold and non-causal elements of the claimed invention. Further, "some weight ought to be given to a persuasively supported statement of one skilled in the art on what was not obvious to him." *In re Lindell*, 385 F.2d 453, 456, 155 USPQ, 521, 524 (CCPA 1967).

The Applicant has demonstrated that the combination of references does not explicitly describe the limitations of claims 17, 33, and 35, or suggest any modifications that might make these limitations obvious, and the Applicant requests that the rejections be removed.

The Applicant notes that only claims 17, 33, and 35 have been rejected as obvious. Claims 18-32, dependent from claim 17, claim 34, dependent from claim 33, and claims 36-48, dependent from claim 35, all include additional subject matter that necessarily limits the independent claims. However, the Office Action provides no analysis stating that the subject matter of any of the dependent claims is obvious. For example, the Applicant submits that the prior art does not describe the future decision or present decision circuits of claim 18. The Applicant respectfully submits that the dependent claims all include subject matter that acts to further distinguish the claimed invention from the prior art references.

The Final Office Action also states that claims 17-48 have been provisionally rejected under the judicially created doctrine of double patenting with respect to copending application 10/077,332, which is a CIP of the instant application. In the event that claims are allowed, the Applicant is willing to file a Terminal Disclaimer.

SUMMARY AND CONCLUSION

It is submitted that for the reasons pointed out above, the claims in the present application clearly and patentably distinguish over the cited references. Accordingly, the Examiner should be reversed and ordered to pass the case to issue.

A check in the amount of $500.00 is enclosed to cover the fee for this Appeal Brief. Authorization is given to charge any deficit or credit any excess to Deposit Account No. 502033.

Respectfully submitted,

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CLAIMS APPENDIX

IN THE CLAIMS:

1-16. Cancelled

17. (Previously Presented) A non-causal channel equalization communication system, the system comprising:

a multi-threshold circuit having an input to accept a non-return to zero (NRZ) data stream, an input to accept threshold values, and outputs to provide a plurality of bit estimates for each NRZ data, responsive to a plurality of voltage threshold levels; and,

a non-causal circuit having inputs to accept the bit estimates from the multi-threshold circuit and an output to supply a first bit value for a current clock cycle in response to comparing a first bit estimate for the current clock cycle, to bit values determined in non-current clock cycles.

18. (Previously Presented) The system of claim 17 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs to accept the bit estimates, the future decision circuit having outputs to supply the first bit estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, determined for a clock cycle prior to the current clock cycle, and the third bit value, determined for a clock cycle subsequent to the current clock cycle, the present decision circuit having an output to supply the first bit

value determined in response to comparing the first bit estimate to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

19. (Original) The system of claim 18 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the NRZ data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the NRZ data stream, an input establishing a second threshold (V0), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the NRZ data stream, an input establishing a third threshold (Vopt), and an output to provide a signal when the NRZ data stream input has an approximately equal probability of being a "0" value as a "1" value.

20. (Original) The system of claim 19 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" if both the second and third bit value are "0" values;

a first bit value of "0" if only one of the second and third bit values is a "0" value; and,

a first bit value of "0" if both the second and third bit values are a "1".

21. (Original) The system of claim 20 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" if both the second and third bit value are "1" values;

a first bit value of "1" if only one of the second and third bit values is a "1" value; and,

a first bit value of "1" if both the second and third bit values are a "0".

22. (Previously Presented) The system of claim 21 wherein the multi-threshold circuit accepts an NRZ data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply threshold values to the multi-threshold circuit in response to FEC corrections and an output to supply a stream of corrected data bits.

23. (Previously Presented) The system of claim 22 wherein the FEC circuit includes a first threshold generator having an inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the first threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "1" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values; and,

wherein the first threshold generator has an output to supply the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

24. (Previously Presented) The system of claim 23 wherein the FEC circuit includes a second threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the second threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "0" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values; and,

wherein the second threshold generator has an output to supply the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

25. (Previously Presented) The system of claim 24 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value; and,

wherein the third threshold generator has an output to supply the third threshold (Vopt) in response to corrections tracked in the first bit when one of the second or third bit values is a "1" value.

26. (Previously Presented) The system of claim 24 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and adjusting the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value.

27. (Original) The system of claim 21 further comprising:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream, the first threshold generator tracking the NRZ data stream inputs when the second and third bit values both equal "1" and maintaining a long-term average of the tracked NRZ data stream inputs, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average.

28. (Original) The system of claim 27 further comprising:

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream input, the second threshold generator tracking the NRZ data stream inputs when the second and third bit values both equal "0" and maintaining a long-term average of the NRZ data stream inputs, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average.

29. (Original) The system of claim 28 further comprising:

a third threshold generator having inputs to accept the first (V1) and second (V0) thresholds, and an output to supply the third threshold (Vopt) responsive to the first and second thresholds.

30. (Original) The system of claim 29 wherein the third threshold generator supplies the third threshold approximately midway between the first and second thresholds.

31. (Original) The system of claim 28 further comprising:

a third threshold generator having an input to accept the NRZ data stream input, the third threshold generator measuring the average voltage of the NRZ data stream and supplying the third threshold (Vopt) at an output in response to the measured average.

32. (Original) The system of claim 21 wherein the multi-threshold circuit receives NRZ training data input;

wherein the non-causal circuit supplies first bit values responsive to the received NRZ training data; and,

the system further comprising:

a training circuit with a memory including predetermined training data, an input to accept the first bit values from the non-causal circuit, the training circuit comparing the received first bit values to the training data in memory, and supplying first, second, and third threshold values at an output in response to the comparisons.

33. (Previously Presented) A non-causal channel equalization communication system, the system comprising:

a multi-threshold circuit having an input to accept a data stream and outputs to provide a plurality of bit estimates for each data, responsive to a plurality of voltage threshold levels; and,

a non-causal circuit having an input to accept the bit estimates from the multi-threshold circuit and an output to supply a first bit value for a current clock cycle in response to comparing a first bit

estimate for the current clock cycle to bit values determined in non-current clock cycles.

34. (Previously Presented) The system of claim 33 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply the first bit estimate and subsequent bit values;

a present decision circuit having inputs to accept the first bit estimate, the subsequent bit values, and prior bit values, the present decision circuit comparing the first bit estimate to both the prior bit values, determined for clock cycles prior to the current clock cycle, and the subsequent bit values, determined for clock cycles subsequent to the current clock cycle, the present decision circuit having an output to supply the first bit value determined in response to comparing the first bit estimate to the prior and subsequent bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the prior bit values.

35. (Previously Presented) A non-causal channel equalization communication system, the system comprising:

a multi-threshold circuit having an input to accept a data stream encoded with forward error correction and an output to provide a plurality of bit estimates for each data, responsive to a plurality of voltage threshold levels;

a non-causal circuit having an input to accept the bit estimates from the multi-threshold circuit and an output to supply a first

bit value for a current clock cycle in response to comparing a first bit estimate for the current clock cycle to bit values determined in non-current clock cycles; and,

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the data stream and correcting first bit values in response to the decoding, the FEC circuit having an output to supply threshold levels to the multi-threshold circuit in response to the FEC corrections.

36. (Previously Presented) The system of claim 35 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs to accept the bit estimates, the future decision circuit having outputs to supply the first bit estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, determined for a clock cycle prior to the current clock cycle, and the third bit value, determined for a clock cycle subsequent to the current clock cycle, the present decision circuit having an output to supply the first bit value determined in response to comparing the first bit estimate to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

37. (Previously Presented) The system of claim 34 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the data stream, an input establishing a second threshold (V0), and an output to supply a signal distinguishing when the data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the data stream, an input establishing a third threshold (Vopt), and an output to provide a signal when the data stream input has an approximately equal probability of being a "0" value as a "1" value.

38. (Previously Presented) The system of claim 37 wherein the future decision circuit supplies a first bit estimate for a data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" if both the second and third bit value are "0" values;

a first bit value of "0" if only one of the second and third bit values is a "0" value; and,

a first bit value of "0" if both the second and third bit values are a "1".

39. (Previously Presented) The system of claim 38 wherein the future decision circuit supplies a first bit estimate for a data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" if both the second and third bit value are "1" values;

a first bit value of "1" if only one of the second and third bit values is a "1" value; and,

a first bit value of "1" if both the second and third bit values are a "0".

40. (Previously Presented) The system of claim 39 wherein the multi-threshold circuit accepts a data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply threshold values to the multi-threshold circuit in response to FEC corrections and an output to supply a stream of corrected data bits.

41. (Previously Presented) The system of claim 40 wherein the FEC circuit includes a first threshold generator having an inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the first threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "1" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values; and,

wherein the first threshold generator has an output to supply the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

42. (Previously Presented) The system of claim 41 wherein the FEC circuit includes a second threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the second threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "0" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values; and,

wherein the second threshold generator has an output to supply the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

43. (Previously Presented) The system of claim 42 wherein the FEC circuit includes a third threshold generator having

inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value; and,

wherein the third threshold generator has an output to supply the third threshold (Vopt) in response to corrections tracked in the first bit when one of the second or third bit values is a "1" value.

44. (Previously Presented) The system of claim 42 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and adjusting the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value.

45. (Previously Presented) The system of claim 39 further comprising:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the data stream, the first threshold generator tracking the data stream inputs when the second and third bit values both equal "1" and maintaining a long-term average of the tracked data stream inputs, the first threshold generator

having an output to supply the first threshold (V1) responsive to the long-term average.

46. (Previously Presented) The system of claim 45 further comprising:

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the data stream input, the second threshold generator tracking the data stream inputs when the second and third bit values both equal "0" and maintaining a long-term average of the data stream inputs, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average.

47. (Previously Presented) The system of claim 46 further comprising:

a third threshold generator having inputs to accept the first (V1) and second (V0) thresholds, and an output to supply the third threshold (Vopt) responsive to the first and second thresholds.

48. (Previously Presented) The system of claim 47 wherein the third threshold generator supplies the third threshold approximately midway between the first and second thresholds.

SYSTEM AND METHOD FOR NON-CAUSAL CHANNEL EQUALIZATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to digital communications and, more particularly, to a system and method for minimizing the effects of inter-symbol interference in a non-return to zero (NRZ) data channel.

2. Description of the Related Art

Fig. 1 is a diagram illustrating a signal recovered from a binary symmetric, non-dispersive channel in the presence of noise (prior art). Conventionally, the signal is filtered with a transfer function matched to the signaling waveform (in this case a one unit step) and thresholded at the voltage level most likely to yield the transmitted bit. To recover the transmitted information, a hard decision must be made on the value of the received bit.

As a function of the filtering process, and sometimes as a result of the transmission process, pulse spreading occurs. That is, the energy associated with a bit spreads to neighboring bits. For small degrees of spreading these effects of this can be limited to the nearest neighbors with modest degradation in performance.

Three basic types of pulse spreading exist. The first possibility is that both the neighboring bits are a zero (no neighboring bits are a one). The second possibility is that only one of the neighboring bits (either the preceding or subsequent bit) is a one. Alternately stated, only one of the neighboring bits is a zero. The third possibility is that both neighboring bits are one. For each of these cases the likelihood of error in

determining a bit value can be minimized if a different thresholds are used for different bit combinations.

Fig. 2 is a diagram illustrating received waveforms that are distorted in response to the inter-symbol interference resulting from energy dispersion (prior art). The value at the output of the filter varies with each bit, and is essentially a random process, due to the non-deterministic nature of the information, and scrambling that is often used in the transmission of NRZ data streams. However, received bits can be characterized with probability density functions, as shown. Without knowledge of the neighboring bits, a single probability density function could be extracted that represents the random behavior of the input over all conditions and all sequences. However, conditional probability density functions can be defined for the three cases mentioned above. Namely, probability density functions can be defined for the cases where there are zero neighboring ones, only one neighboring one, and two neighboring ones.

If the bit value decision process could be made using the knowledge of the decision made on the preceding decoded bit, and with a measurement of a subsequent decoded bit, then the corresponding probability density function could be selected to make a more accurate decision on the current bit decision. However, the cost and accuracy of conventional analog-to-digital (A/D) conversion circuits make such a solution impractical.

The degree of dispersion exhibited by a channel, and hence the separation of the conditional probability density functions, varies in response to a number of fixed and variable factors. Effective dispersion mitigation techniques must therefore be easily optimized to the channel

and somewhat adaptive to changes in the channel due to aging, temperature changes, reconfiguration, and other possible influences.

It would be advantageous if inter-symbol interference caused by energy dispersion in a received NRZ data channel could be minimized.

It would be advantageous if the bit decision thresholds could be modified to take account of the dispersed energy in the neighboring bits in the NRZ data stream.

SUMMARY OF THE INVENTION

Many communication channels exhibit temporal spreading of the signaling waveform when propagating over long distances or over non-linear media. This phenomenon is not effectively addressed by traditional linear equalization techniques due to the non-causal nature of the impairment. A method is presented to reduce the effects of pulse spreading on hard-decision error rate in communication systems affected by this problem. The method utilizes multiple decision thresholds for each data bit. Post-processing of the multiple decision data is employed to reduce the data to a single hard decision per bit. The multiple data thresholds are adjusted for optimal mitigation of the spreading effect.

The proposed approach to this problem is to perform multiple decisions on every bit with a threshold for each of the above-mentioned conditional probability density functions. The multiple decision data is stored for several bit times, to allow a calculation to be made on the succeeding bits. This calculation is then used to select the threshold most appropriate given the estimated neighbor values. The refined decision is output from the device and fed-forward to be used in processing of subsequent bits.

Accordingly, a method is provided for non-causal channel equalization in a communications system. The method comprises: establishing a first threshold (V1) to distinguish a high probability "1" first bit estimate; establishing a second threshold (V0) to distinguish a high probability "0" first bit estimate; establishing a third threshold (Vopt) to distinguish first bit estimates between the first and second thresholds; receiving a non-return to zero (NRZ) data stream. Typically, the data stream is encoded with forward error correction (FEC). The method further comprises: comparing a first bit estimate to a second bit value received prior to the first bit; comparing the first bit estimate to a third bit value received subsequent to the first bit; in response to the comparisons, determining the value of the first bit.

Establishing a third threshold (Vopt) includes: distinguishing NRZ data stream inputs below the first threshold and above the third threshold as a "0" if both the second and third bits are "1" values, as a "1" if only one of the second and third bits is a "1" value, and as a "1" if both the second and third bit values are a "0"; and, distinguishing NRZ data stream inputs above the second threshold and below the third threshold as a "1" if both the second and third bits are a "0" value, as a "0" if only one of the second and third bits is a "0" value, and as a "0" is both the second and third bit values are a "1".

In one aspect the method further comprises: following the determination of the first bit values, FEC decoding the first bit values; and, using the FEC corrections of the first bit values to adjust the first, second, and third threshold values. Alternately, an averaging process is used to track and maintain the threshold values.

Additional details of the above-described method, and a non-causal channel equalization communication system are provided below.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram illustrating a signal recovered from a binary symmetric, non-dispersive channel in the presence of noise (prior art).

Fig. 2 is a diagram illustrating received waveforms that are distorted in response to the inter-symbol interference resulting from energy dispersion (prior art).

Fig. 3 is a schematic block diagram of the present invention non-causal channel equalization communication system.

Fig. 4 is a graph illustrating the thresholds established by the multi-threshold circuit.

Fig. 5 is a schematic block diagram detailing the FEC circuit of Fig. 3.

Fig. 6 is a schematic block diagram illustrating an alternate aspect of the system, where an averaging circuit is used instead of the FEC circuit.

Figs. 7a and 7b are a schematic block diagram and associated truth table of the non-causal circuit of Figs. 3 and 6 in greater detail.

Fig. 8 is a schematic block diagram of the first threshold generator of Fig. 5, used to illustrate the counter embodiment.

Fig. 9 is a graph illustrating the operation of the threshold generators as embodied in Fig. 8.

Figs. 10a and 10b are flowcharts illustrating the present invention method for non-causal channel equalization in a communications system.

Fig. 11 is a flowchart illustrating an alternate embodiment of Step 412 of Fig. 10.

Fig. 12 is a flowchart illustrating the training aspect of the present invention method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 is a schematic block diagram of the present invention non-causal channel equalization communication system. The system 100 comprises a multi-threshold decision circuit 102 having an input on line 104 to accept a non-return to zero (NRZ) data stream, and an input on line 106 to accept threshold values. The multi-threshold decision circuit 102 has outputs on line 108 to provide bit estimates responsive to a plurality of voltage threshold levels. A non-causal circuit 110 has inputs on line 108 to accept the bit estimates from the multi-threshold decision circuit 102. The non-causal circuit 110 compares a current bit estimate (a first bit) to bit values decisions made across a plurality of clock cycles. The non-causal circuit 110 has an output to supply a bit value decision for the current bit estimate determined in response to the non-causal bit value comparisons.

The non-causal circuit 110 includes a present decision circuit 112, a future decision circuit 114, and a past decision circuit 116. The future decision circuit has inputs connected to the mutli-threshold circuit

outputs on line 108. The future decision circuit 114 has outputs to supply the first bit estimate and the third bit value (as explained below). The present decision circuit 112 has inputs to accept the first bit estimate, the third bit value, and a second bit value from the past decision circuit 116. The present decision circuit 112 compares the first bit estimate in the data stream to the second bit value received prior to the first bit estimate, represented as being supplied from the past decision circuit 116 on line 118. The present decision circuit 112 also compares the first bit estimate to the third bit value received subsequent to the first bit estimate, represented as being from the future decision circuit 114 on line 120. The present decision circuit 112 has an output on line 122 to supply a first bit value determined in response to comparing the first bit estimates to the second and third bit values.

Fig. 4 is a graph illustrating the thresholds established by the multi-threshold circuit. The following discussion should be considered in light of both Figs. 3 and 4. The multi-threshold circuit 102 includes a first comparator 124 having an input to accept the NRZ data stream on line 104, an input connected on line 106a to establish a first threshold (V1), and an output on line 108a to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "1" bit value. A second comparator 126 has an input on line 104 to accept the NRZ data stream, an input on line 106b to establish a second threshold (V0), and an output on line 108b to supply a signal distinguishing when NRZ data stream input has a high probability of being a "0" bit value. More literally, the second comparator 126 supplies a "0" when the NRZ data stream input on line 104 has a high probability of being a "0".

A third comparator 128 has an input on line 104 to accept the NRZ data stream, an input on line 106c to establish a third threshold (Vopt), and an output on line 108c to provide a signal when the NRZ data stream input has an approximately equal probability of being a "0" value as a "1" value. Distinguishing between a "1" and a "0" is a process that is performed by the non-causal circuit 110.

In some aspects of the system, the multi-threshold circuit 102 accepts an NRZ data stream encoded with forward error correction (FEC). Then, the system 100 further comprises a forward error correction (FEC) circuit 130 having an input on line 122 to receive the (first) bit values from the non-causal circuit 110. The FEC circuit 130 decodes the incoming data stream and corrects bit value in response to the decoding. The FEC circuit 130 has an output on line 106, specifically lines 106a, 106b, and 106c, to supply threshold values to the multi-threshold circuit 102 in response to the FEC corrections. The FEC circuit 130 has an output on line 132 to supply a stream of corrected data bits.

The multi-threshold circuit 102 and the non-causal circuit 110 work together perform a non-causal analysis, regardless of whether the system incorporates the FEC circuit 130. When the multi-threshold circuit 102 receives a NRZ data stream input below the third threshold (Vopt) and above the second threshold (V0), the present decision circuit (of the non-causal circuit 110) responds by supplying a (first) bit value of "1" on line 122, if both the second and third bit values are "0" on lines 118 and line 120, respectively. Otherwise, the present decision circuit 112 supplies a bit value of "0", if only one of the second and third bit values is a "0", or if both the second and third bit values are a "1". When the multi-threshold circuit 102 receives a NRZ data stream input above the third

threshold and below the first threshold, the present decision circuit 112 responds by supplying a bit value decision of "0" if both the second and third bit values are "1". The present decision circuit 112 supplies a bit value decision of "1" if only one of the second and third bits is a "1" value, or if both the second and third bit values are a "0".

Fig. 5 is a schematic block diagram detailing the FEC circuit 130 of Fig. 3. The FEC circuit 130 includes a decoder 200 having an input to accept the bit value on line 122 and an output to supply the stream of corrected data bits on line 132. The FEC circuit 130 also includes a first threshold generator 202 having an input on line 132 to accept the stream of corrected data bits. The first threshold generator 202 also has an input to accept the (first) bit values from the non-causal circuit on line 122. The first threshold generator 202 tracks the number of corrections in the first bit when the first bit value is determined to be a "0" and the second and third bits are both "1" values. That is, lines 122 and 132 are compared. Likewise, the first threshold generator 202 tracks the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values. The first threshold generator 202 has an output on line 106a to supply the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

The FEC circuit 130 also includes a second threshold generator 204 having an input on line 132 to accept the stream of corrected data bits. The second threshold generator 204 has an input to accept the bit values from the non-causal circuit on line 122. The second threshold generator 204 tracks the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third

bits are both "0" values. The second threshold generator 204 tracks the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values. The second threshold generator 204 has an output on line 106b to supply the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

The FEC circuit 130 includes a third threshold generator 206 having an input on line 132 to accept the stream of corrected data bits. The third threshold generator 206 has an input on line 122 to accept bit values from the non-causal circuit. The third threshold generator 206 tracks the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value. Alternately, corrections could be tracked of when the first bit is determined to be a "1" value and only one of the second and third bits is a "1" value. The third threshold generator 206 has an output on line 106c to supply the third threshold (Vopt) in response to corrections tracked in the first bit when one of the second or third bit values is a "1" value. The threshold generators 202-206 can supply an analog voltage on line 106, or a digital signal that is translated into an analog voltage at the multi-threshold circuit.

In another aspect of the system 100, the FEC circuit 130 third threshold generator 206 just tracks the number of corrections in the first bit when the first bit is determined to be a "1" value, without regard to the previous or subsequent bit values, and adjusts the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value. Alternately, third threshold generator 206 tracks the number of corrections in the first bit when the first bit is determined to be

a "0" value, without regard to the previous or subsequent bit values, and adjusts the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "0" value. That is, the Vopt threshold is generated without non-causal analysis.

Fig. 6 is a schematic block diagram illustrating an alternate aspect of the system, where an averaging circuit is used instead of the FEC circuit. The multi-threshold circuit 102 and the non-causal circuit 110 are the same as explained in the description of Fig. 3. In this aspect of the system 600, long-term averages are maintained to minimize processing in the determination of the threshold settings. An averaging circuit 601 is shown to "hold" the threshold generators described below. However, it should be understood that the threshold generators could alternately be included as part of the multi-threshold circuit 102 or the non-causal circuit 110. A first threshold generator 602 has an input to accept the output of the non-causal circuit (first bit value) on line 122. The first threshold generator 602 also has an input connected on line 104 to accept the NRZ data stream input. The first threshold generator 602 tracks the NRZ data stream inputs (in the clock period associated with the first bit) when the second and third bit values both equal "1" and maintains a long-term average of the tracked NRZ data stream input. That is, an averaged is maintained of the NRZ data stream voltage when the second and third bit values equal "1". The first threshold generator 602 supplies the first threshold (V1) responsive to the long-term average.

Likewise, a second threshold generator 604 has an input connected to the output of the non-causal circuit 110 on line 122 and an input to accept the NRZ data stream input on line 104. The second threshold generator 604 tracks the NRZ data stream inputs when the

second and third bit values both equal "0" and maintains a long-term average of the NRZ data stream inputs. The average NRZ data stream voltage is kept when the second and third bits have a "0" value. The second threshold generator 604 supplies the second threshold (V0) on line 106b responsive to the long-term average.

In the long-term average scenario, processing is even further reduced with respect to a third threshold generator 606. The third threshold generator 606 has inputs on lines 106a and 106b to accept the first (V1) and second (V0) thresholds, respectively. The third threshold generator 606 has an output on line 106c to supply the third threshold (Vopt) responsive to the first and second thresholds. There are many different algorithms that can be used to select the third threshold value. In one aspect of the system 600, the third threshold generator 606 supplies the third threshold approximately midway between the first and second thresholds. This threshold can be further adjusted to account for asymmetrical noise distribution. Note that the present invention system 600 may incorporate FEC processing downstream from the non-causal circuit 110 (not shown). The threshold generators 602-606 can supply an analog voltage on line 106, or a digital signal that is translated into an analog voltage at the multi-threshold circuit.

In another aspect of the system 600, the third threshold generator accepts the NRZ data stream input, shown as a dotted line 104. The third threshold generator 606 maintains the average voltage, or a digital representation of the average voltage, on the NRZ data stream input. Note, this is a measurement of the NRZ data stream without regard to non-causal analysis, or the analysis of bit values. The third threshold generator 606 supplies the third threshold (Vopt) at an output

on line 106c in response to the measured average. The third threshold can be set the measured average, for example. Note in this aspect, the input lines 106a and 106b are not needed. With pseudorandom scrambling it assumed that the average voltage is a result of an equal number of "0" and "1" bits being received on line 104. This method of generating the third threshold is very effective when the noise distribution is symmetrical.

In some aspects of the system, the threshold values are initialized using training data. The training data is a stream of predetermined NRZ data, for example, an alternating pattern of "0s" and "1s". The multi-threshold circuit 102 receives NRZ training data input on line 104 and processes it as described above. The non-causal circuit 110 supplies first bit values on line 122 responsive to the received NRZ training data as described above. The system 600 further comprises a training circuit 610 with a memory 612 including the predetermined training data. The training circuit 610 has an input to accept the first bit values from the non-causal circuit 110 on line 122. The training circuit 610 compares the received first bit values to the training data in memory. This comparison operation would be equivalent to the explanation of Fig. 5, where the FEC circuit compares corrected data to the first data bit values, and will not be repeated in the interest of brevity. The training circuit 610 supplies first, second, and third threshold values at an output on lines 106a, 106b, and 106c, respectively, in response to the comparisons. Also, as above, the training circuit would include threshold generators (not shown). Note that a training circuit, although not shown, could also be used in the system of Fig. 3. After initialization, either the

FEC process (Fig. 3), or the averaging process (Fig. 6), can be used to further correct the threshold values as described above.

Figs. 7a and 7b are a schematic block diagram and associated truth table of the non-causal circuit 110 of Figs. 3 and 6 in greater detail. Fig. 7a represents only one of many designs that can be used to embody the invention. The future decision circuit 114 has inputs connected to the outputs of the first, second, and third comparators of the multi-threshold circuit on lines 108a, 108b, and 108c, respectively. These three lines correspond to the thresholds shown in Fig. 4. The future decision circuit 114 passes the third comparator signal through on line 120c. This signal is called the third bit value. The future decision circuit 114 performs AND and OR operations using AND circuit 301, AND circuit 302, and OR circuit 303. Delays of one clock cycle are added using flip-flops 304 and 306. When the NRZ data stream input is less than V0, the estimates on line 120a and 120b are "0,0", respectively. When the NRZ data stream input is between Vopt and V0, the estimates on lines 120a and 120b are "0,1", respectively. When the NRZ data stream input is between Vopt and V1, the estimates on lines 120a and 120b are "1,0", respectively. When the NRZ data stream input is above V1, the estimates are lines 120a and 120b are "1,1", respectively. The combination of lines 120a and 120b is called the first bit estimate.

The past decision circuit 116 delays the first bit value on line 122 one clock cycle to supply the second bit value on line 118. Again, a D flip-flop 308 is used for the delay.

The present decision circuit 112 has inputs connected to the future decision circuit outputs to accept the first bit estimate and third bit value on lines 120a, 120b, and 120c, respectively. The present decision

circuit 112 supplies a first bit value by comparing the first bit estimate to situations when the second and third bit decision values are both "1", when the second and third bit value decisions are both "0", and when only one of the second and third bit value decisions is a "1". To accomplish these above-stated goals, AND circuits 310 through 318 are employed. Note that AND circuits 316 and 318 have one inverted input and that 310 has an inverted output (NAND). Also used are OR and XOR gates 320 through 326. Again, alternate circuit designs can accomplish the same functions. More important is the relationship between the signal inputs and signal outputs.

Fig. 7b is a truth table illustrating the operation of the present decision circuit 112 of Fig. 7a. The non-causal circuit 110 of the present invention systems 100 and 600 can be implemented using many different combinations of circuits. More critical is the actual task performed. This task is more clearly defined in light of the truth table diagram.

The first four lines in the table illustrate the case where the NRZ data input, at a clock period associated with a first bit, is below V0. The first bit value is made in comparison to the four different combinations of the second and third bit values. Likewise, the second four lines in the table illustrate the case where the NRZ data input, at a clock period associated with a first bit, is above V0 and below Vopt. The third set of four lines in the table illustrates the case where the NRZ data input is above Vopt, but below V1. The last set of four lines in the table illustrates the case where the NRZ data input is above V1.

Functional Description

Returning to Figs. 3 and 6, in some aspects of the system 100/600, the NRZ input signal is buffered (not shown). The NRZ data signal is provided to the multiple threshold comparators 124 through 126. In some aspects of the system 100/600 circuits, not shown, a timing recovery circuit is used at the output of the comparators on lines 108a through 108c. The timing recovery circuit generates a clock and sample signal from the received data. The sample signal is synchronized to the center of the data bit. In this implementation, a method for offsetting the sample point is provided to compensate device or channel specific anomalies.

The non-causal circuit 110 is used as a high performance decision device prior to FEC decoding in the system 100. FEC decoding provides additional information on the validity of the estimates made by the non-causal circuit 110 as a by-product of the error correction procedure. This information can be processed and used to optimize the decision points of multi-threshold circuit 102. Error rate information on the relative probability of a ones ("1s") error vs. a zeros ("0s") error is collected for the four cases of the probability density function (PDF). Specifically:

PDF 1) P(errorred one | no neighboring 1s)
P(errorred zero | no neighboring 1s)

PDF 2) P(errorred one | preceding neighbor 1)
P(errorred zero | preceding neighbor 1)

PDF 3) P(errorred one | following neighbor 1)
P(errorred zero | following neighbor 1)

PDF 4) P(errorred one | two neighboring 1s)
P(errorred zero | two neighboring 1s)

Since most FEC encoded systems are also scrambled to insure a 50% mark ratio, statistical data for each of the three cases can be reduced to a ratio. Each threshold can be adjusted to achieve the ones/zero ratio that provides the best fit for the channel in use. In many cases this will be ~50%. For cases in which dispersion is symmetric, PDF 2 and PDF 3 are combined to a single statistic.

With respect to the threshold generators of Fig. 5, one embodiment of the system would be to use eight counters and four sets of feedback control signals for the purpose of dispersion mitigation, V1±, V2±, V3±, and V4±. A three-set mode could be achieved by combining the statistics in condition 2 and 3 in the third threshold generator. A description of the four conditions that define each statistic set follows:

Condition 1: 0 before, 0 after error;
Condition 2: 1 before, 0 after error;
Condition 3: 0 before, 1 after error; and,
Condition 4: 1 before, 1 after error.

Fig. 8 is a schematic block diagram of the first threshold generator 202 of Fig. 5, used to illustrate the counter embodiment. For each of the four conditions, registers separately tally the number of "1s" errors and the number of "0s" errors. The errors are the difference between the raw and corrected data. Separate V1± pins are also provided for each condition. Statistics are collected, and feedback pins toggled, when only one error is detected in the three-bit sequence described below. Statistics gathering is inhibited when data is known to be unreliable, such as during an uncorrectable event, loss of frame, or loss of clock.

The statistics circuit 350 examines bit value combinations where the pervious and subsequent bit value decisions are a "1". When a "0" error is detected, the "0" counter 352 is toggled with signal +V4 on line

354. When a "1" error is detected, the "1" counter 356 is toggled with signal –V4 on line 358. A summing circuit 360 reads the counters 352 and 356 and provides the first threshold (V1) on line 106a in response. The second and third threshold circuits would function in a similar manner. The summing circuit can supply an analog voltage or a digital signal that is converted into an analog voltage by the multi-threshold circuit.

Fig. 9 is a graph illustrating the operation of the threshold generators as embodied in Fig. 8. The statistics circuit examines corrected sequences, where "ER" represents an error. For example, an error in the sequence " 1 0 1" generates a –V4 toggle, while an error in the sequence "1 1 1" generates a +V4 toggle.

The above-described equalization process has a significant effect on the overall performance of the channel. Modern optical channels employ a variety of dispersion management techniques. Dispersion management may be employed to various levels of complexity, and hence cost. The system of the present invention can be performed on a per fibre basis, or per lambda basis. In addition, management may be static or adaptive. In any case, it is expected that the signal will be left with a residual effect that may be addressed by the technique described above.

Figs. 10a and 10b are flowcharts illustrating the present invention method for non-causal channel equalization in a communications system. This method generally corresponds to Fig. 3. Although the method (and the methods of Figs. 11 and 12, below) is depicted as a sequence of numbered steps for clarity, no order should be inferred from the numbering unless explicitly stated. It should be understood that some of these steps may be skipped, performed in parallel, or performed without the requirement of maintaining a strict

order of sequence. The method starts at Step 400. Step 401a establishes a first threshold (V1) to distinguish a high probability "1" first bit estimate. Step 401b establishes a second threshold (V0) to distinguish a high probability "0" first bit estimate. Step 401c establishes a third threshold (Vopt) for first bit estimates between the first and second thresholds. Step 402 receives a non-return to zero (NRZ) data stream input. Step 403 supplies the first bit estimate for comparison in response to distinguishing the NRZ data stream input at the first, second, and third thresholds. Step 404 compares the first bit estimate in the data stream to a second bit value received prior to the first bit. Step 406 compares the first bit estimate to a third bit value received subsequent to the first bit. Step 408, in response to the comparisons, determines the value of the first bit.

In some aspects of the method, establishing a third threshold (Vopt) to distinguish first bit estimates between the first and second thresholds in Step 401c includes substeps. Step 401c1 (not shown) distinguishes NRZ data stream inputs below the first threshold and above the third threshold as a "0" if both the second and third bits are "1" values, as a "1" if only one of the second and third values is a "1" value, and as a "1" if both the second and third bits are a "0" value. Step 401c2 (not shown) distinguishes NRZ data stream inputs above the second threshold and below the third threshold as a "1" if both the second and third bits are a "0" value, as a "0" if only one of the second and third values is a "0" value, and as a "0" if both the second and third bits are a "1" value.

In some aspects, receiving a non-return to zero data stream in Step 402 includes receiving a non-return to zero data stream encoded

with forward error correction (FEC). Then, the method comprises further steps. Step 410, following the determination of the first bit values, FEC decodes the first bit values. Step 412 uses the FEC corrections of the first bit values to adjust the first, second, and third threshold values.

In some aspects of the method, using the FEC corrections of the first bit values to adjust the first, second, and third threshold values in Step 412 includes substeps. Step 412a tracks the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "1" values. Step 412b tracks the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values. Step 412c adjusts the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

In some aspects, using the FEC corrections of the data stream to adjust the first, second, and third threshold values in Step 412 includes additional substeps. Step 412d tracks the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "0" values. Step 412e tracks the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values. Step 412f adjusts the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

In some aspects, using the FEC corrections of the data stream to adjust the first, second, and third threshold values in Step 412 includes additional substeps. Step 412g tracks the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value. Step 412h tracks the

number of corrections in the first bit when the first bit is determined to be a "1" value and only of the second and third bits is a "1" value. Step 412i adjusts the third threshold (Vopt) in response to corrections tracked when only one of the second or third bit values is a "1" value.

As an alternative to Steps 412g through 412i, Step 412j tracks the number of corrections in the first bit when the first bit is determined to be a "1" value (alternately a "0" value). Step 412k adjusts the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value (alternately a "0" value). Note, this process does not consider the preceding or subsequent bits.

Fig. 11 is a flowchart illustrating an alternate embodiment of Step 412 of Fig. 10. Steps 400 through 408 are the same as in Fig. 10a and will not be repeated in the interest of brevity. The method generally corresponds to Fig. 6 and uses some alternate steps from those shown in Figs 10a and 10b. Step 414 tracks the NRZ data stream inputs when the second bit value equals the third bit value. Step 416 maintains long-term averages of the tracked NRZ data stream inputs. Step 418 adjusts the first and second thresholds in response to the long-term averages.

In some aspects of the method, tracking the NRZ data stream inputs when the second bit value equals the third bit value in Step 414 includes substeps (not shown). Step 414a tracks the NRZ data stream inputs when the second and third bits both have "1" values. Step 414b tracks the NRZ data stream inputs when the second and third bits have "0" values.

In other aspects, maintaining long-term averages of the tracked NRZ data stream inputs in Step 416 includes substeps (not shown). Step 416a creates a first average of the NRZ data stream inputs

when the second and third bits are both "1" values. Step 416c creates a second average of the NRZ data stream inputs when the second and third bits are both "0" values.

In some aspects, adjusting the first and second thresholds in response to the long-term averages in Step 418 includes substeps (not shown). Step 418a adjusts the first threshold (V1) in response to the first average. Step 418b adjusts the second threshold (V0) in response to the second average.

Some aspects of the invention include a further step. Step 420 adjusts the third threshold (Vopt) in response to adjusting the first (V1) and second (V0) thresholds in Step 418a and 418b, respectively. For example, the third threshold can be set to approximately midway between the first and second thresholds. Alternately, Step 420 includes substeps not shown. Step 420a measures the average NRZ data stream input voltage. That is, the voltage is measured constantly with regard to temporal analysis of the bit values. Step 420b sets the third threshold in response to the measured average.

Fig. 12 is a flowchart illustrating the training aspect of the present invention method. These steps could be used prior to Steps 401a of either Fig. 10a or Fig. 11. The method starts at Step 500. Step 502 receives predetermined training data prior to receiving the (nondeterministic) NRZ data stream (Step 402 of either Fig. 10a or Fig. 11). Step 504 determines first bit values from the training data. This process would equivalent to Step 403 through Step 408 of Figs. 10a and 11. Step 506 corrects the determined first bit values with the predetermined training data. Step 508 uses the corrections of the first bit values to adjust the first, second, and third threshold values.

A system and method have been provided for non-causally adjusting a NRZ data stream channel. Because inter-symbol dispersion is a non-causal impairment, the estimation algorithms are more effective when based upon iteratively collected data. The degree of iteration affects the performance of the circuit and is selected based upon the implementation tradeoffs. It is expected that those skilled in the art could implement the collection of such data. Although exemplary analysis algorithms using only the preceding and subsequent bits have been explicitly described, the present invention would obviously apply to algorithms using one than one preceding or subsequent bit value. Other embodiments and variations of the invention will occur to those skilled in the art.

WE CLAIM:

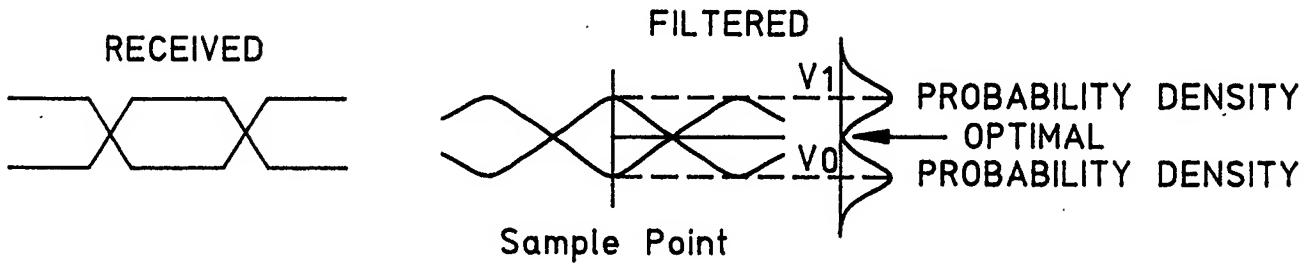


FIG. 1 (PRIOR ART)

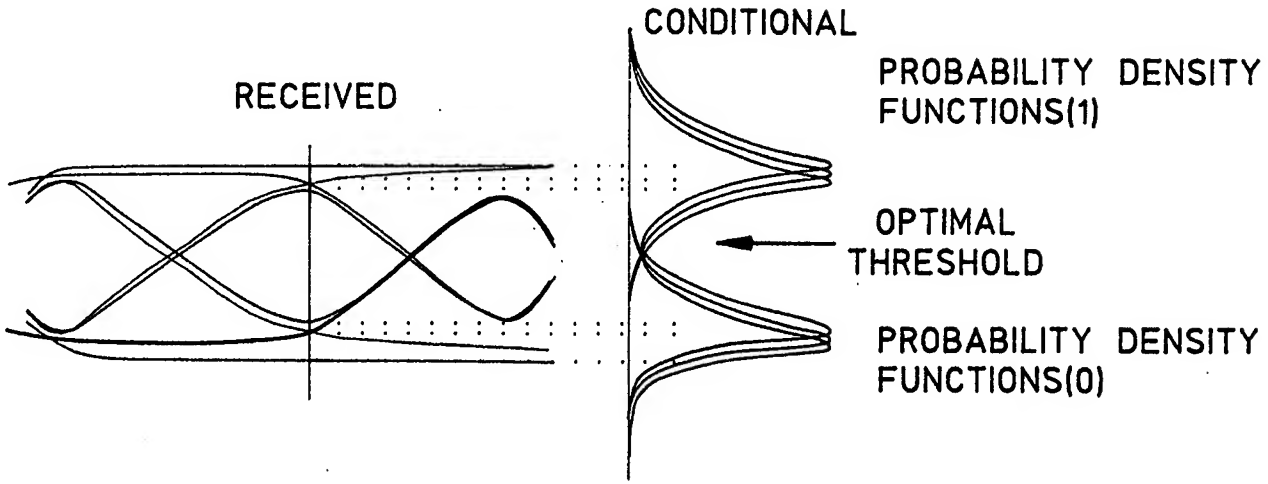


FIG. 2 (PRIOR ART)

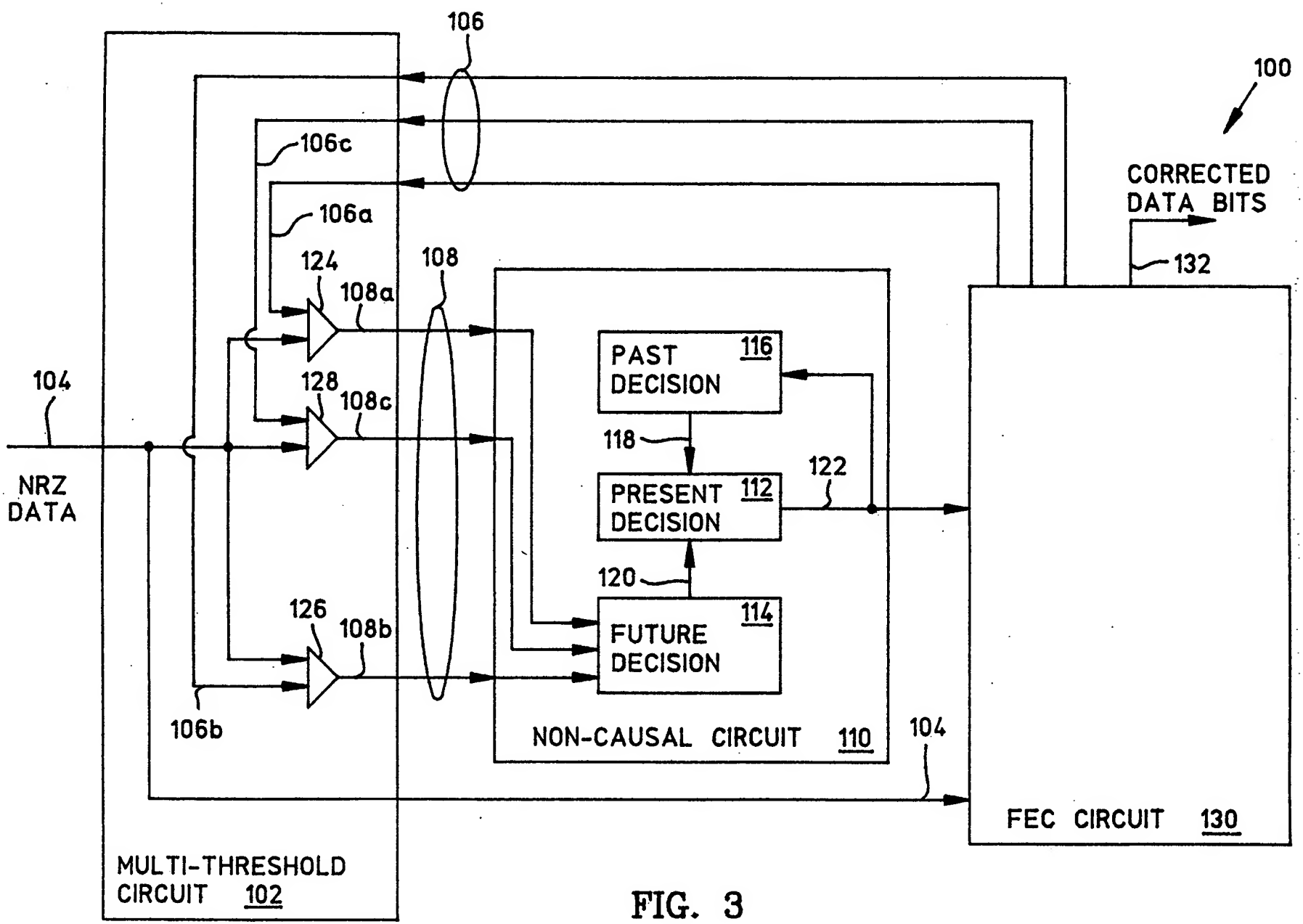

106
100
106c
CORRECTED
DATA BITS
106a
124
108
132
108a
104
128
108c
PAST
116
DECISION
118
122
NRZ
DATA
PRESENT
112
DECISION
120
126
108b
114
FUTURE
DECISION
106b
NON-CAUSAL CIRCUIT 110
104
FEC CIRCUIT 130
MULTI-THRESHOLD
CIRCUIT 102

FIG. 3

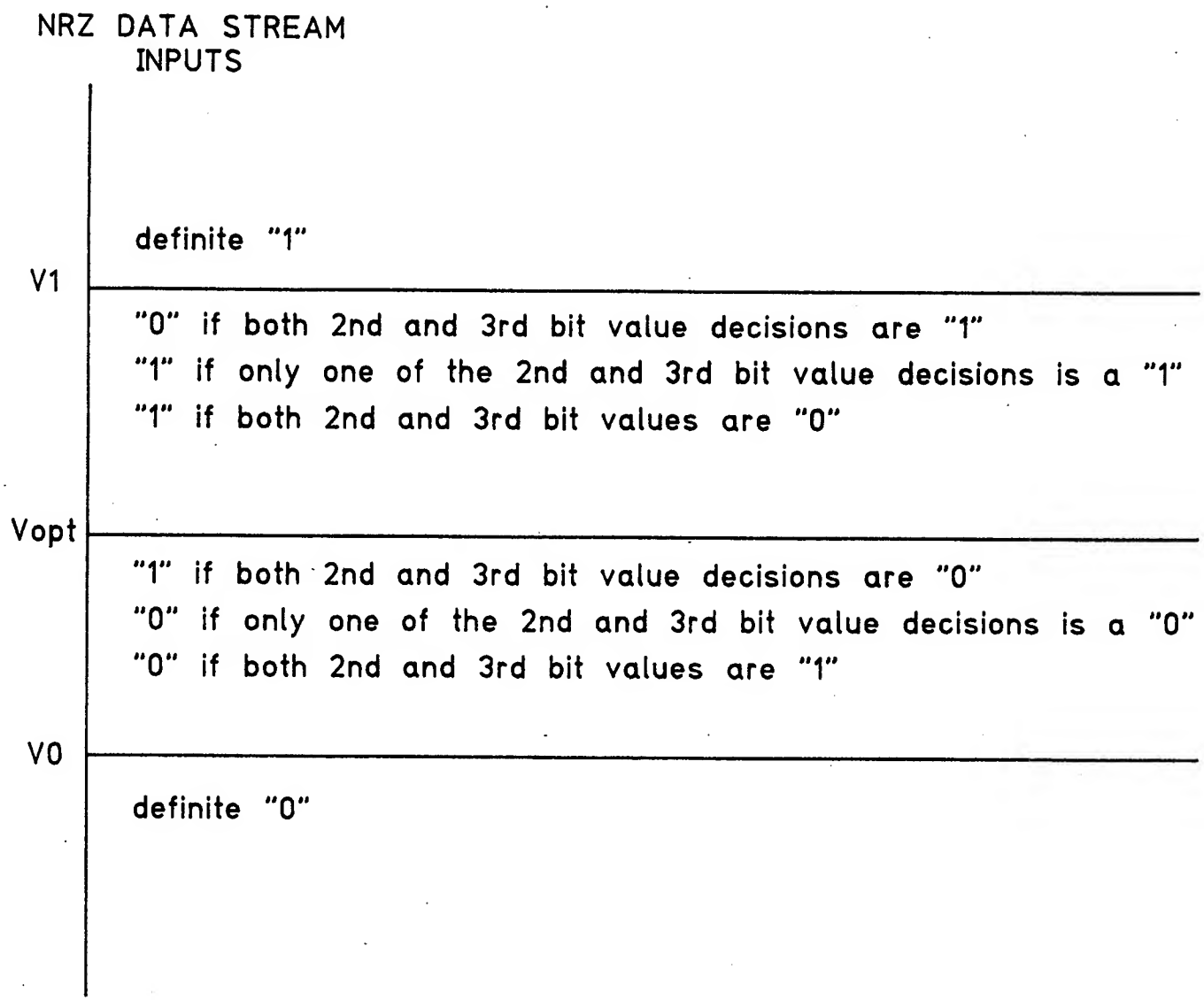

NRZ DATA STREAM
INPUTS
definite "1"
V1
"0" if both 2nd and 3rd bit value decisions are "1"
"1" if only one of the 2nd and 3rd bit value decisions is a "1"
"1" if both 2nd and 3rd bit values are "0"
Vopt
"1" if both 2nd and 3rd bit value decisions are "0"
"0" if only one of the 2nd and 3rd bit value decisions is a "0"
"0" if both 2nd and 3rd bit values are "1"
V0
definite "0"

FIG. 4

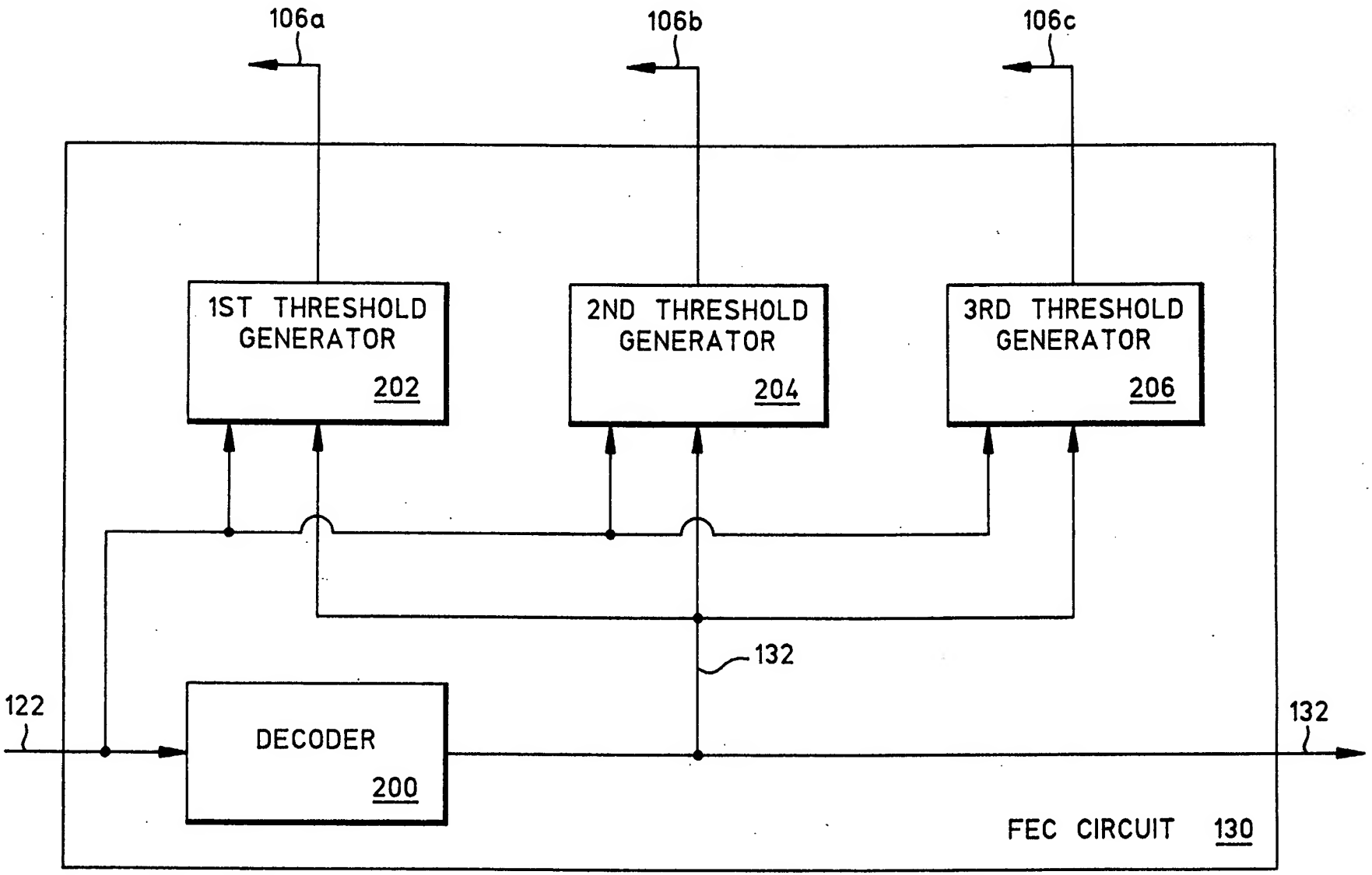

106a
106b
106c
1ST THRESHOLD GENERATOR
202
2ND THRESHOLD GENERATOR
204
3RD THRESHOLD GENERATOR
206
132
122
DECODER
200
132
FEC CIRCUIT 130

FIG. 5

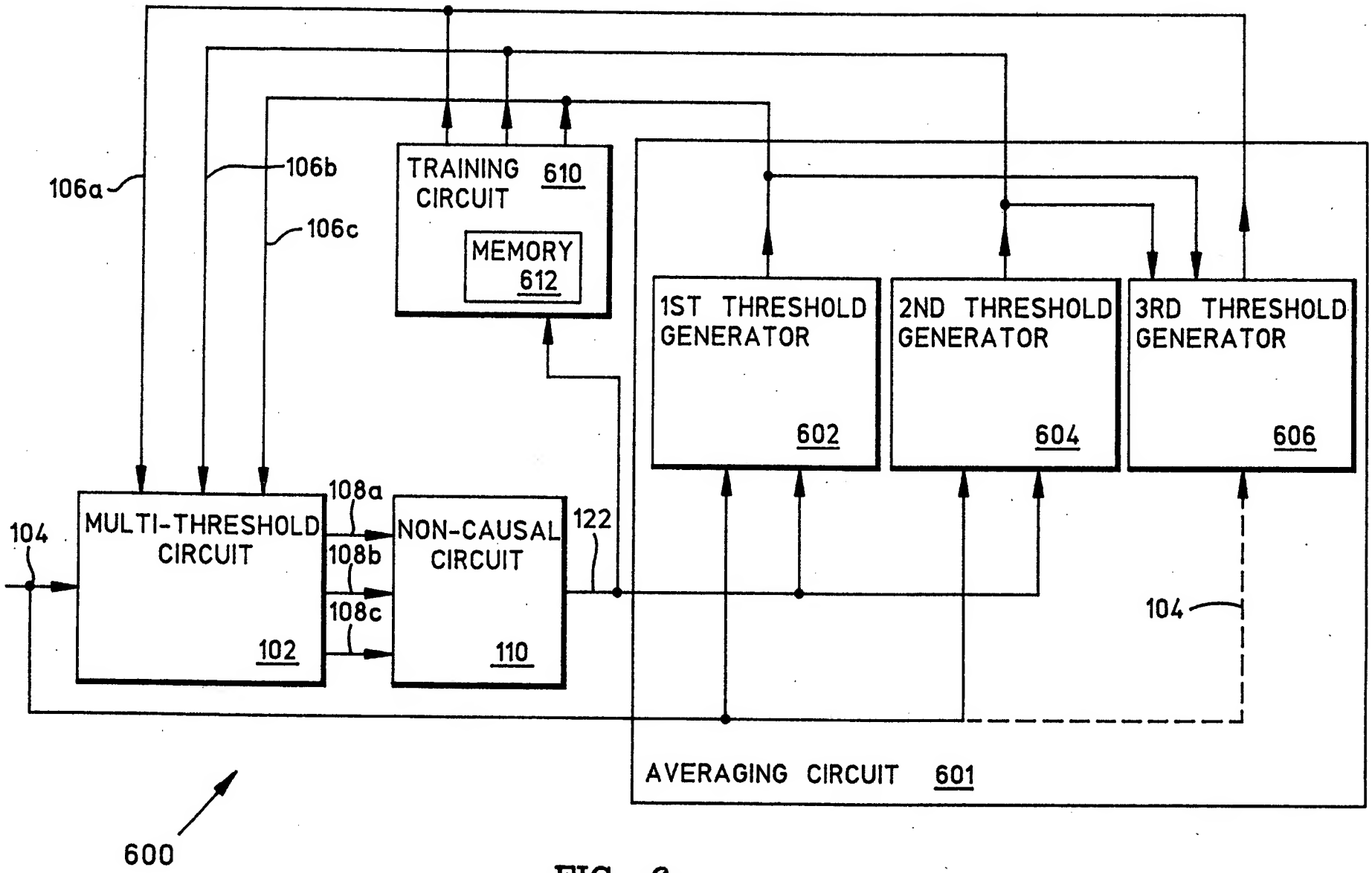

106a
106b
106c
TRAINING CIRCUIT 610
MEMORY 612
1ST THRESHOLD GENERATOR 602
2ND THRESHOLD GENERATOR 604
3RD THRESHOLD GENERATOR 606
104
MULTI-THRESHOLD CIRCUIT 102
108a
108b
108c
NON-CAUSAL CIRCUIT 110
122
104
AVERAGING CIRCUIT 601
600

FIG. 6

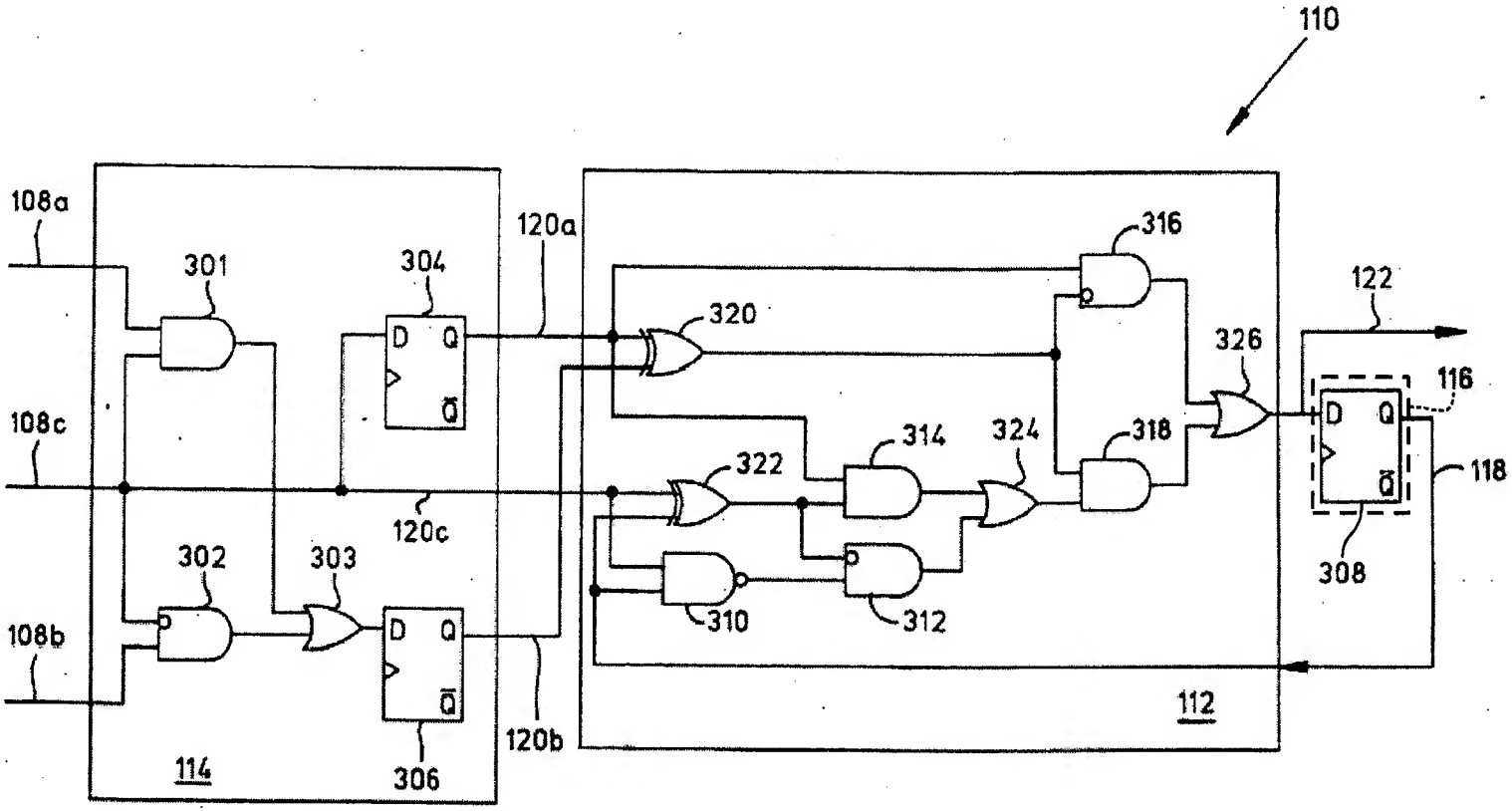

110
108a
108c
108b
301
302
303
304
D
Q
Q̄
120a
120c
120b
114
306
320
322
310
312
314
324
316
318
326
122
116
118
308
112

FIG. 7A

FIRST BIT ESTIMATE Line 120a	120b	2ND BIT Value	3RD BIT Value	1ST BIT Value
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

FIG. 7B

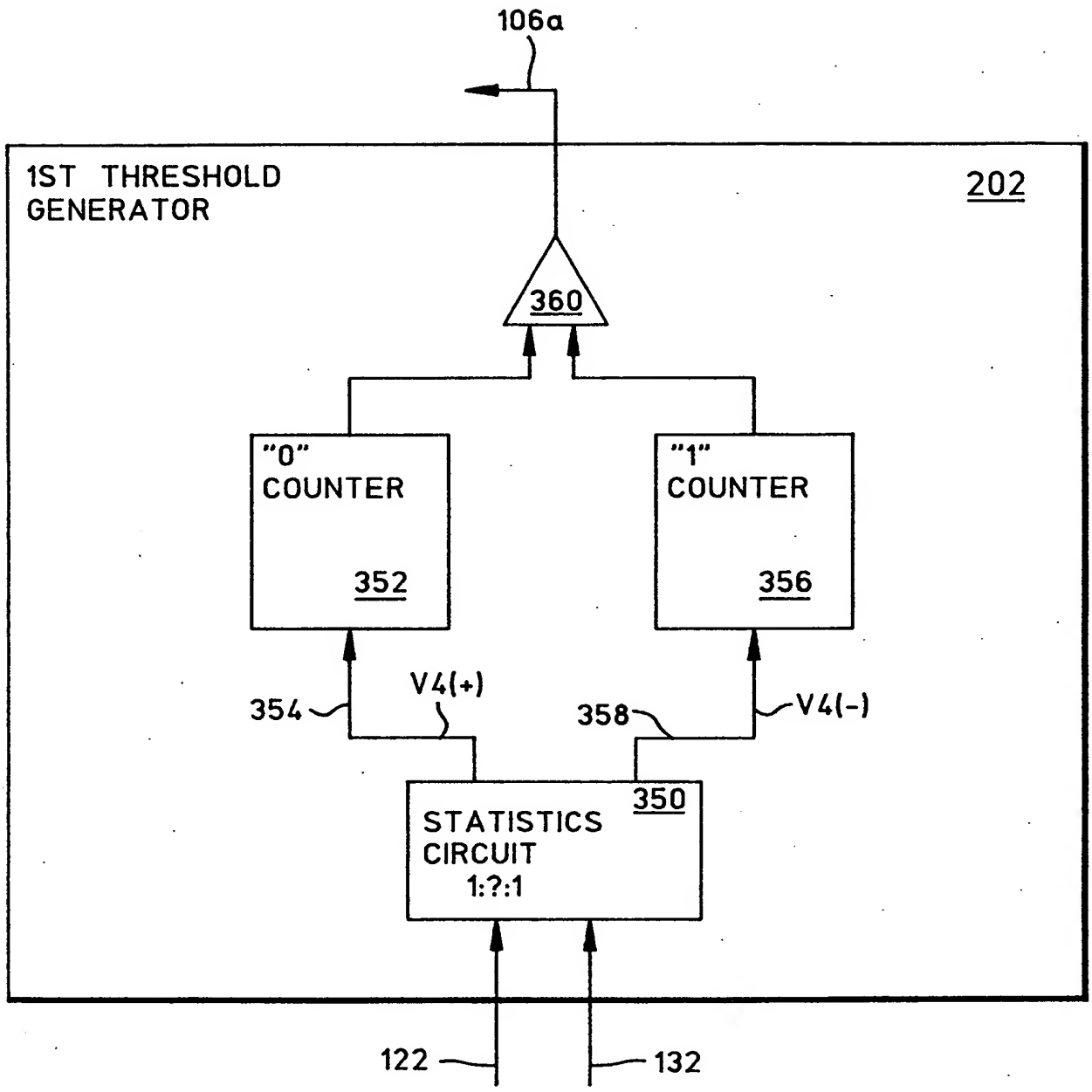

106a
1ST THRESHOLD GENERATOR
202
360
"0" COUNTER
352
"1" COUNTER
356
354
V4(+)
358
V4(-)
350
STATISTICS CIRCUIT
1:?:1
122
132

FIG. 8

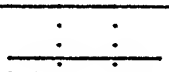
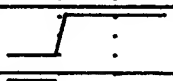
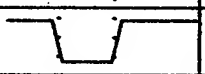
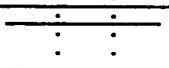
Only One Correction per 3 bit sequence Error in the center bit					
Corrected Sequence	Graphic	Affected Counter		Action on Feedback	
OK-ER-OK		0 cntr	1 cntr	-	+
0 0 0		Cond 1 0 inc		V1 Toggle	
0 0 1		Cond 2 0 inc		V2 Toggle	
0 1 0			Cond 1 1 inc		V1 Toggle
0 1 1			Cond 2 1 inc		V2 Toggle
1 0 0		Cond 3 0 inc		V3 Toggle	
1 0 1		Cond 4 0 inc		V4 Toggle	
1 1 0			Cond 3 1 inc		V3 Toggle
1 1 1			Cond 4 1 inc		V4 Toggle

FIG. 9

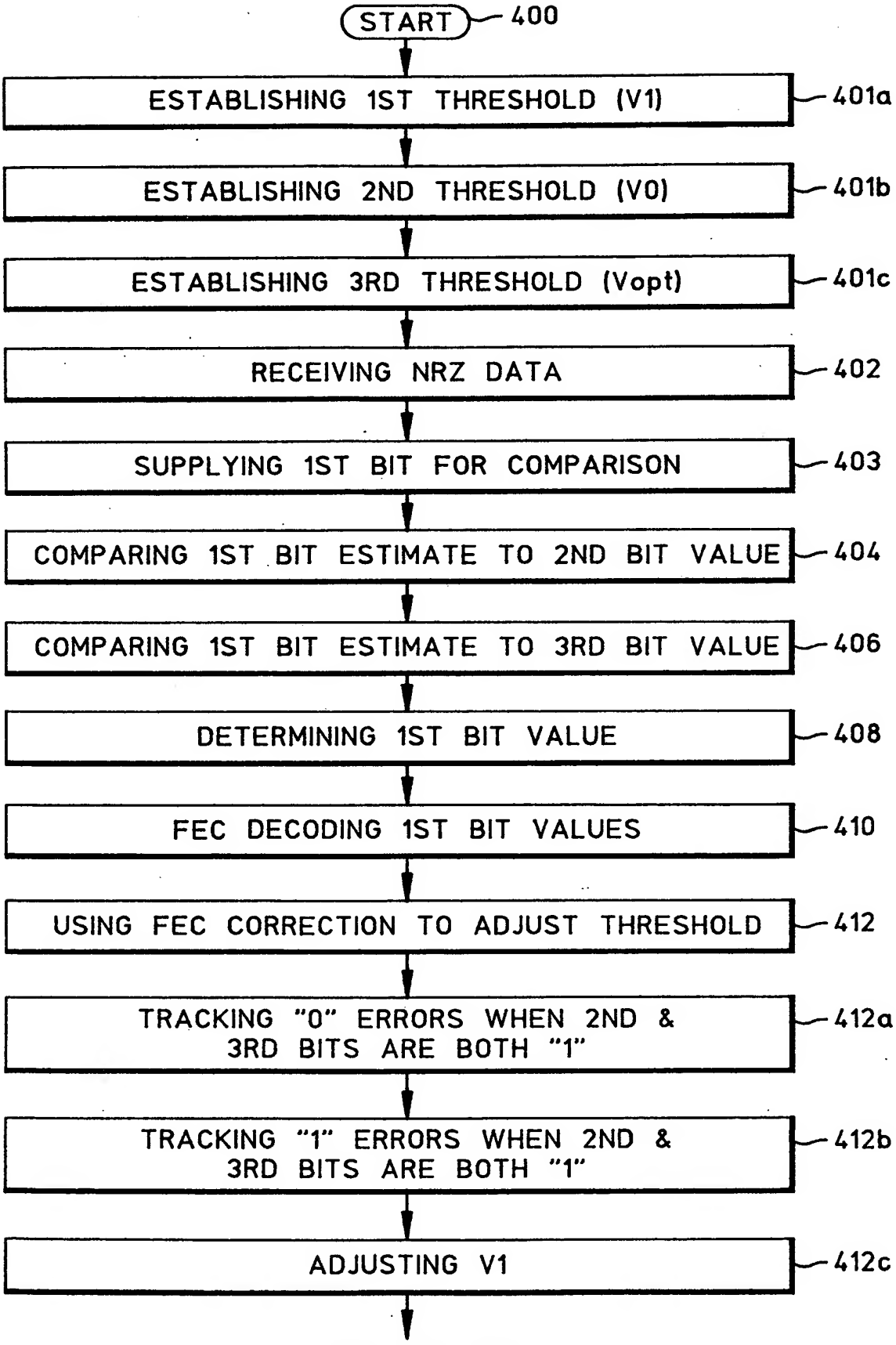

START
400
ESTABLISHING 1ST THRESHOLD (V1)
401a
ESTABLISHING 2ND THRESHOLD (V0)
401b
ESTABLISHING 3RD THRESHOLD (Vopt)
401c
RECEIVING NRZ DATA
402
SUPPLYING 1ST BIT FOR COMPARISON
403
COMPARING 1ST BIT ESTIMATE TO 2ND BIT VALUE
404
COMPARING 1ST BIT ESTIMATE TO 3RD BIT VALUE
406
DETERMINING 1ST BIT VALUE
408
FEC DECODING 1ST BIT VALUES
410
USING FEC CORRECTION TO ADJUST THRESHOLD
412
TRACKING "0" ERRORS WHEN 2ND & 3RD BITS ARE BOTH "1"
412a
TRACKING "1" ERRORS WHEN 2ND & 3RD BITS ARE BOTH "1"
412b
ADJUSTING V1
412c
TO FIG. 10B

FIG. 10A

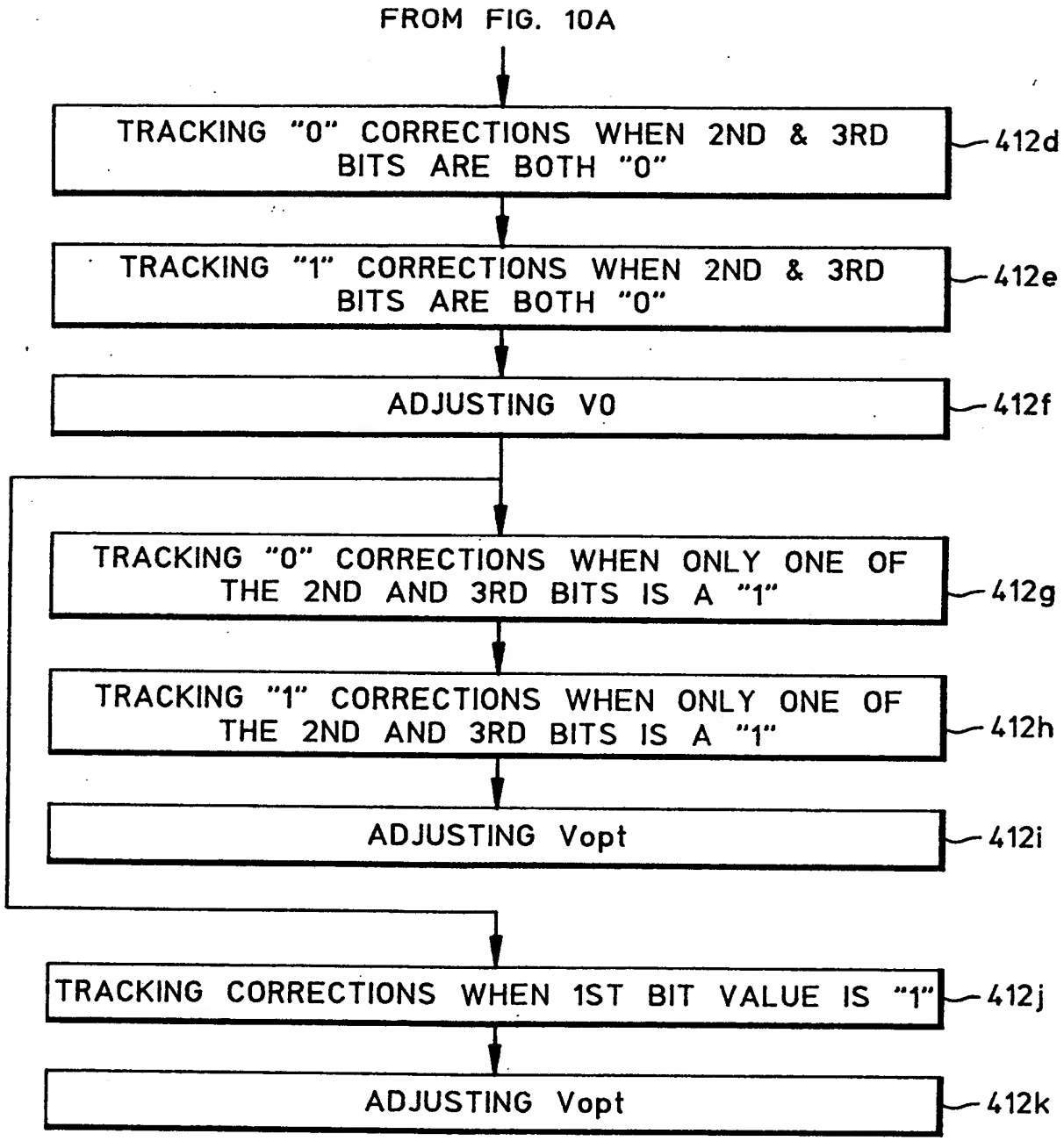

FROM FIG. 10A
TRACKING "0" CORRECTIONS WHEN 2ND & 3RD BITS ARE BOTH "0"
412d
TRACKING "1" CORRECTIONS WHEN 2ND & 3RD BITS ARE BOTH "0"
412e
ADJUSTING V0
412f
TRACKING "0" CORRECTIONS WHEN ONLY ONE OF THE 2ND AND 3RD BITS IS A "1"
412g
TRACKING "1" CORRECTIONS WHEN ONLY ONE OF THE 2ND AND 3RD BITS IS A "1"
412h
ADJUSTING Vopt
412i
TRACKING CORRECTIONS WHEN 1ST BIT VALUE IS "1"
412j
ADJUSTING Vopt
412k

FIG. 10B

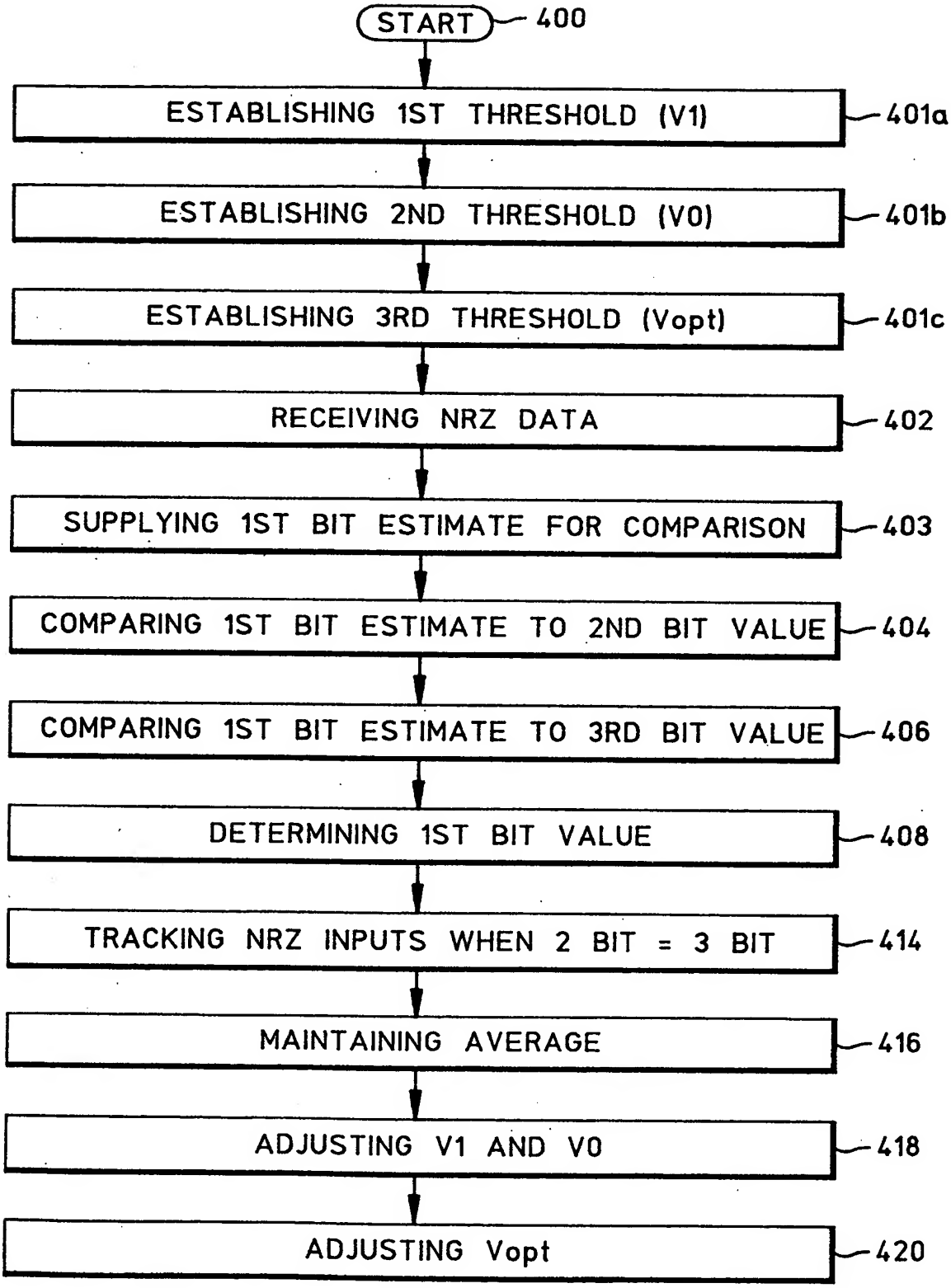

START
400
ESTABLISHING 1ST THRESHOLD (V1)
401a
ESTABLISHING 2ND THRESHOLD (V0)
401b
ESTABLISHING 3RD THRESHOLD (Vopt)
401c
RECEIVING NRZ DATA
402
SUPPLYING 1ST BIT ESTIMATE FOR COMPARISON
403
COMPARING 1ST BIT ESTIMATE TO 2ND BIT VALUE
404
COMPARING 1ST BIT ESTIMATE TO 3RD BIT VALUE
406
DETERMINING 1ST BIT VALUE
408
TRACKING NRZ INPUTS WHEN 2 BIT = 3 BIT
414
MAINTAINING AVERAGE
416
ADJUSTING V1 AND V0
418
ADJUSTING Vopt
420

FIG. 11

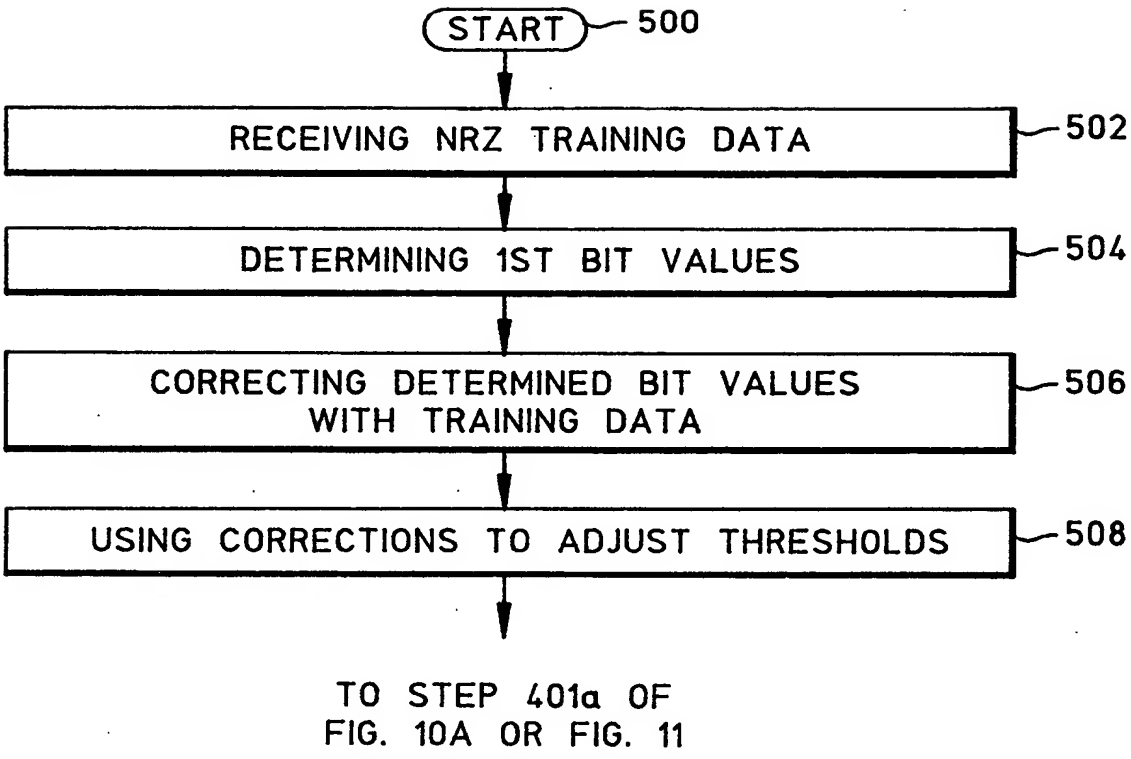

START
500
RECEIVING NRZ TRAINING DATA
502
DETERMINING 1ST BIT VALUES
504
CORRECTING DETERMINED BIT VALUES WITH TRAINING DATA
506
USING CORRECTIONS TO ADJUST THRESHOLDS
508
TO STEP 401a OF FIG. 10A OR FIG. 11

FIG. 12

Attachment C
In Application Serial No. 10/020,426
Filed December 7, 2001

DECLARATION OF OSWIN SCHREIBER UNDER 37 CFR §1.132

I, Oswin Schreiber, Ph.D., hereby declare as follows:

1. My residence address is 12949 Angosto Way, San Diego, CA 92128.

2. My degrees include:

University of Mainz, PhD in Physics 1985; and

University of Mainz, Master in Physics 1980.

3. A list of some of my publications is enclosed as Attachment D.

4. From 1985 until 1987, I worked at Toshiba LTD, in Munich, with the Sales Department.

5. From 1987 until 1988, I worked at Siemens, in Munich, as the Product Marketing Manager of Optical Data Links.

6. From 1988 until 2000, I worked at AT&T ME/Lucent Microelectronics, in Munich. My responsibilities included Marketing Manager for High Speed Physical Layer Devices, Distributor Manager, and Sales Engineer.

7. Since September 1st, 2000 I have been employed by Applied Micro Circuits Corp. (AMCC), 6290 Sequence Drive, San Diego, CA 92121. My title at AMCC is Senior Product Marketing Scientist. My

responsibilities Product Marketing functions, coordinating R&D efforts, leading new product ideas to marketable products representing AMCC's products in the optical market space, and publishing articles.

8. I have read the claims for the patent application in question, Castagnozzi et al., Serial Number 10/020,426 (the Applicant). I have read the relevant parts of the Office Action dated December 9, 2004, where 17, 33, and 35 have been rejected as obvious with respect to Andresen (US 3,670,304) and Abe (US 5,781,588). In summary, it is my opinion that neither of the cited references, even when combined makes the invention of claims 17, 33, or 35 obvious.

9. In claims 17, 33, and 35, and as shown in Fig 3, the Applicant recites two claims elements: a multi-threshold decision circuit and a non-causal circuit. Claim 35 includes the additional claim element of an FEC circuit. The multi-threshold decision circuit accepts an input and supplies a plurality of bit estimates for each input symbol. That is, the incoming data symbol is simultaneously compared to several different thresholds. The non-causal circuit accepts these bit estimates and compares one of the bit estimates (the first bit estimate) to bit decisions for other clock cycles. In response to the comparison, the non-causal circuit generates the current (first) clock cycle bit value.

With respect to claim 35, the FEC circuit accepts the bit values, performs FEC corrections, and uses these corrections to adjust the threshold levels of the multi-threshold decision circuit, to minimize the number of FEC corrections that are required.

10. Andresen describes a magnetic tape reading device that accepts an analog signal with a non-predetermined amplitude. Andresen compares the input to thresholds for the purpose of creating a hard-limited

digital input from the analog signal. Threshold decisions are made at amplitude sensor 14, and OR gate 18 to create the hard-limited signal on line 27 of Fig. 1. This signal is fed to the data detector for the purpose of generating data pulses, clock pulses, and as an input to the feedback circuitry that is used to generate the limiter threshold values.

11. There are several differences between Andresen and claims 17, 33, and 35. The purposes of the inventions are different. Andresen is primarily concerned with creating digital data from a magnetic tape analog input signal. The problem to be solved by Andresen is that the analog input voltage levels fluctuate. That is, Andresen is trying to generate accurate digital values from a binary values embedded in an analog signal. The purpose of the Applicant's invention is to generate accurate digital values by eliminating the interference resulting from the voltage levels of neighboring symbols.

Generally, Andresen uses a feedback circuit to adjust the limiter threshold values. Simultaneously, Andresen converts the limited signal to impulse (narrow) pulses, decouples the impulse pulses from phase changes, generates a clock signal, and in response to clock and impulse pulses, generates data pulses. In contrast, the Applicant chooses not to hard-limit the input signal, but rather creates multiple bit estimates of what an input symbol might represent using parallel threshold comparators. The Applicant's non-causal circuit, knowing the sequence of bit decisions, selects a threshold value, and therefore a bit estimate, that optimally accounts for voltage error inherent in the sequence. For example, if the previous and subsequent data values are both "1", the non-causal circuit compensates for the effect of a generally higher voltage level at the time of the current clock bit decision.

12. There are profound differences between Andresen and the Applicant's circuitry. First, Andresen does not create several bit estimates by comparing an input symbol to various threshold levels. In the Applicant's invention, the bit estimates are a preliminary decision made as to the binary value of the input symbol. That is, each input symbol generates a plurality of parallel binary values, either a "1" or a "0". Each estimate is a decision as the whether the input symbol is a "1" or "0". Andresen's limited signal is not a decision of the input symbol's binary value, although the limited signal may closely track the data value that is ultimately made further on in the process. Rather, the limited signal is simply a processed version of the input signal. A high voltage input (see "A", Fig. 2) is emphasized (limited) to be a maximum voltage (see "E", Fig. 2). Likewise, a low voltage is processed (limited) to be a minimum voltage. It should be noted that when the analog input amplitude is too small, no processing is performed, and the analog input is passed on line 27 unprocessed. In this circumstance, Andresen's limiter does not create a signal that even looks like digital data. If Andresen's limited signal (line 27) were to be considered to be an estimate, then the estimates are only made in some circumstances, when the input signal amplitudes are large enough. The fact that Andresen's hard-limited signal looks like a digital signal (in some circumstances) should not be confused with the fact that Andresen's circuitry makes no determination of the binary symbol values on line 27. The binary symbol value determinations are made later in the process, in Andresen's data detector.

Further, the hard-limiting process does not provide a plurality of bit estimates for each input symbol, but rather only a single signal per input symbol (per tape track). Line 72 (Fig. 3) shows that there is only a single output for each tape track. That is, there is only a single hard-limited signal

for each input data stream. Thus, Andresen does not describe a circuit or combination of circuits that perform the function of the Applicant's multi-threshold decision circuit.

13. Second, Andresen does not perform a non-causal analysis. Andresen never makes a bit decision dependent based upon the bit values decisions made in other clock cycles. Thus, Andresen does not describe a circuit, or combination of circuits that perform the function of the Applicant's non-causal circuit. The Office Action states that Andresen's data detector functions as a non-causal circuit. Andresen's data detector might be said to generate a current clock cycle bit value in response to the hard-limited signal input. However, this decision is made without the consideration of bit decisions made in other clock cycles. As I mentioned above, Andresen converts the hard-limited signal to impulse (narrow) pulses, decouples the impulse pulses from phase changes, generates a clock signal, and in response to clock and impulse pulses, generates data pulses. The circuit has no inputs to accept decision data made for other clock periods. The Office Action, at the beginning of page 6, states that a current bit estimate D is compared to "reference decisions R1 and R2 made across a plurality of clock cycles; Note; bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles". While I am not entirely sure of the Examiner's point, it is clear that R1 and R2 are not bit values that are determined for non-current clock cycles. Rather, R1 and R2 are shown to be constant amplitude waveforms in Fig. 3. Andresen describes R1 and R2 as reference levels (col. 8, ln. 46-49).

14. Abe describes a variety of FSK demodulation circuits. As is conventional with such circuits, the carrier signal is amplified if it is close to the noise floor, and attenuated (amplified to a lesser degree) if the carrier

signal or in-band spurious signals are relatively large in signal strength. Also, as is conventional, the input signal is down -converted to an IF band, further down -converted to baseband to recover the FM (baseband) spectrum. Then, the FM spectrum is converted to a digital signal. The binary data can be represented in return-to-zero (RZ), return-to-bias (RB), NRZ or other formats. The digital data is recovered using a threshold (bit-state) detector. In one embodiment mentioned in the Office Action (Fig. 37), the point of novelty appears to be that an analysis of the BER can be used to adjust the thresholds used by the bit-state detector to make bit decisions.

15. There are several differences between the Abe invention and the invention of claims 17, 33, and 35. As with Andresen, the differences primarily stem from the entirely different uses to which the inventions are put. Abe's bit-state detector must compensate for errors associated with the input carrier frequency, errors in the LO frequency, variations in input power, the generation of in-band mixer spurs, and errors associated with the demodulation frequency (typically a phase-locked loop). All these potential errors contribute to the digital signal that is detected by the bit-state detector. While Abe does describe the use of BER data to "tune" the bit-state detector thresholds, Abe does not describe circuitry that generates a plurality of bit estimates for each input symbol, or perform a non-causal analysis of bit decisions.

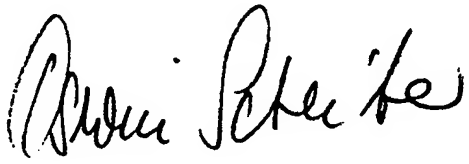
16. I have been asked to state whether I, as an expert in the field, would have been motivated to combine the Abe and Andresen inventions. I have summarized the Abe and Andresen circuitry above, and noted distinctions between the prior art references and the claimed invention. However, the differences between the Abe and Andresen inventions are also quite substantial. At the highest level of abstraction, it is unlikely that I

would look to an RF receiver AGC control circuit to make modification to a tape drive reader. I would consider these types of inventions to be in different fields of art, that rarely cross-pollinate, due to the difference in problems being solved. At the lowest level of abstraction, both inventions compare an input signal to a threshold level, and generate a bit decision. These are very common circuit functions. However, the different uses of the comparator circuits mitigate against any kind of combination. Andresen describes the use of a comparison threshold for hard-limiting an analog tape drive input. This limiting circuit appears to have no applicability to Abe's bit-state detector. Abe does not hard-limit the input to his bit-state detector. If the Examiner is correct in stating that there is indeed a motivation to combine there references, then it must be true that there is motivation to combine any two communication devices. If that were true, I see no point in creating a test for motivation to combine.

17. I have also been asked to consider whether the combination of the Abe and Andresen inventions would result in all the components of the claimed invention, regardless of whether an expert would have realistically sought to combine these inventions. I have mentioned above that neither the Abe nor the Andresen inventions describe the elements of a multi-threshold circuit, which create a plurality of bit estimates for each input symbol. Further, neither Abe nor Andresen describe a non-causal circuit that accepts the bit estimates and creates a bit value for the current clock cycle in response to comparing the bit estimates to bit decisions made in other clock cycles. Without these two components, the claimed invention cannot be practiced. Thus, even if an expert combined every relevant feature from the Abe and Andresen inventions, the result could not be the Applicant's invention.

18. In summary, my opinion is that the cited prior art does not teach the key aspects of the claimed invention, whether considered separately, or in combination. Further, the combination does not suggest any kind of synergistic leap to the claimed invention, as neither reference even discusses the issue of non-causal analysis, much less a circuit to enable such a function.

19. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.



____01/14/05_____ _____

Date Oswin Schreiber

Oswin M. Schreiber

1/13/2005

Attachment D
In Application Serial No. 10/020,426
Filed December 7, 2001

PUBLICATIONS OR OTHER MAJOR MEDIA:

Throughout his career, Dr. Schreiber has authored several vital and germane articles that continue to be extensively used by other leading scientists and researchers in his field (being cited over 330 times). Examples of Dr. Schreiber's authorship of scholarly articles in the field, in professional journals are as follows: (not all listed)

1. Article entitled; "***40-Gbit/s nets call for process shift***," Planet Analog, The EE Times Community (27 Sept. 2004).
2. Article entitled; "***Cost-effectively Designing for 10 Gbit and Beyond in the MAN***," The EE Times (2004).
3. Article entitled; "***OC-768: Jumping Physical Design Hurdles***," The EE Times and CommsDesign (CMP) (29 Aug. 2002).
4. Article entitled; "***40-Gb/s Circuits Built from a 120-GHz f_T SiGe Technology***," The IEE Journal of Solid-State Circuits, Vol. 37, No. 9. (Sept. 2002).
5. Article entitled; "***Diverse Integration a Key Enabler***," The EE Times (06 Aug 2001).
6. Article entitled; "***Optical Communications 40-Gbit/s nets call for process shift***," The Technology Network and The EE Times (13 Apr 2001).
7. Article entitled; "***The Asterix Spectrometer at Lear***," The Nuclear Instruments and Methods in Physics Research, Elsevier Science Publisher A286 (1990) 76-98.
8. Article entitled; "***Antiproton annihilation at rest in nitrogen and deuterium gas***," Physical Review C. Nuclear Physics (Dec. 1989).
9. Article entitled; "***Antiproton-Proton Annihilation at Rest into $\pi+\pi-\pi'$ and $\pi+\pi-\pi$ and the Quark Line Rule***," The Zeitschrift fur Physik C (19 Oct 1989).
10. Article entitled; "***First Observation of K X-Rays from pp Atoms****," The Physics Letters (18 July 1985).
11. Article entitled; "***Protonium Spectroscopy and Identification of P-Wave and S-Wave Initial States of pp Annihilations at Rest with the Asterix Experiment at Lear***," The Physics' at Lear with Low-Entergy Culled Antiprotons, Plenum Publishing Corporation (1984).
12. Article entitled; "***Protonium Spectroscopy and Identification of P-Wave and S-Wave Initial States of pp Annihilations at Rest with the Asterix Experiment at Lear***," The European Organization for Nuclear Research, (01 Oct. 1982).
13. Article entitled; "***A study of pp Interactions at Rest in a H2 Gas Target at Lear***," European Organizaitro for Nuclear Research (29 Aug. 1980).